

# AN119: Calculating Settling Time for Switched Capacitor ADCs

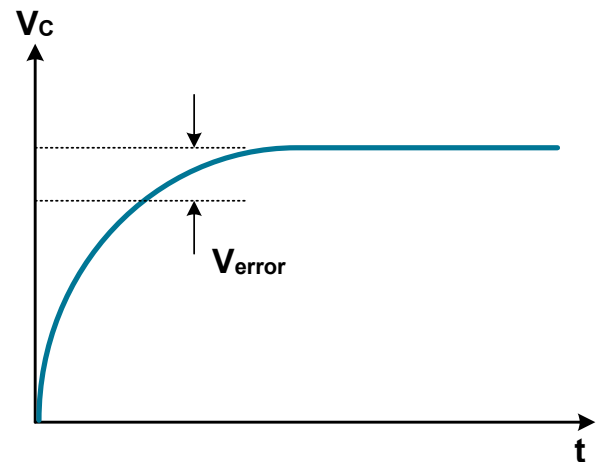
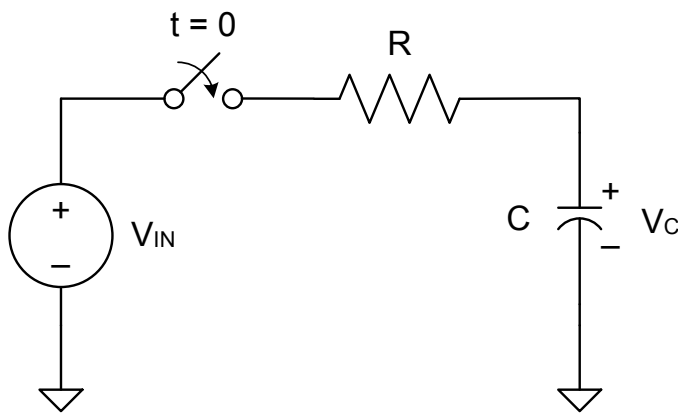


Many of the Silicon Labs EFM8 and C8051 devices feature an on-chip SAR analog-to-digital converter (ADC).

These ADCs use a sample capacitor that is charged to the voltage of the input signal and used by the SAR logic to perform its data conversion. Due to the ADC's sample capacitance, input impedance, and the external input circuitry, there will be a settling time required for the sample capacitor to assume the measured input signal voltage. This application note describes a method for calculating the required settling time for good ADC measurements and methods to achieve settling time requirements.

## KEY POINTS

- The application must allot for settling time for both the on-chip ADC circuitry and the off-chip input circuitry (e.g., anti-alias filter).
- The minimum settling time for the ADC input circuitry is 1.5  $\mu$ s.
- A Thevenin equivalent of the input circuitry is used to estimate the required settling time for the desired accuracy.



## 1. Equivalent Circuit

In order to calculate the estimated settling time, we present an equivalent circuit that approximates the impedance and capacitance of the ADC tracking circuit (i.e., the analog multiplexer, transmission gates, parasitic capacitance, sample capacitance, etc.). An equivalent circuit that approximates these parameters in lumped elements is shown in the figure below. The input signal will typically be filtered through some external input circuitry as determined by the system designer. Most often this will include an anti-alias filter connected to the input pin of the device. The analog multiplexer routes the input signal from the input pin to the ADC. As a conservative estimate, the impedance and capacitance is equivalent to a 5 k $\Omega$  resistor and 10 pF capacitor in series. Note this is a simplified representation of the ADC circuit in tracking mode.

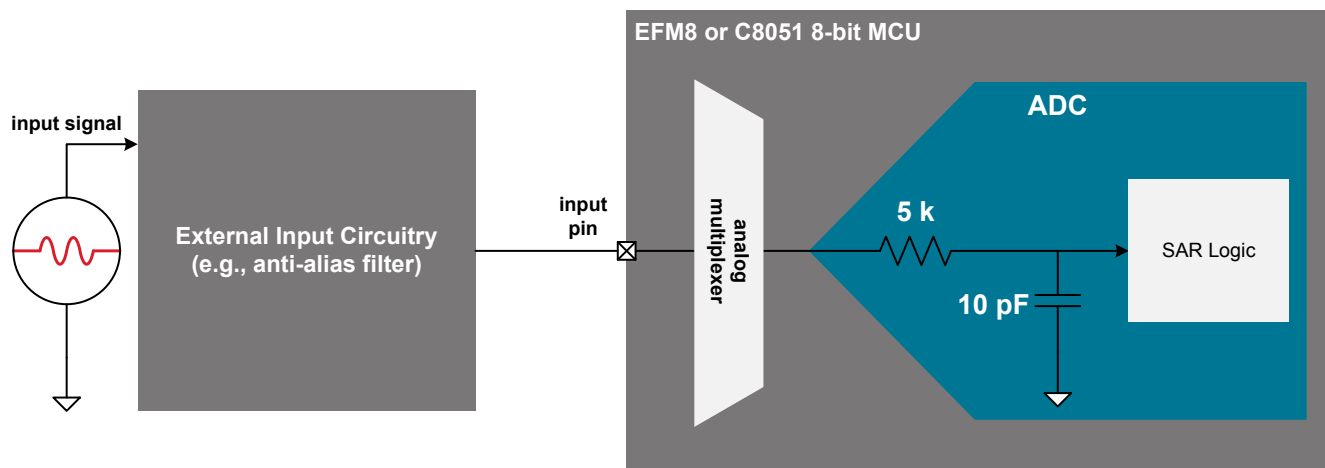


Figure 1.1. Equivalent ADC Circuit for Estimating Settling Time

### 1.1 Differential Ended Measurement

The figure below illustrates the equivalent tracking mode approximation in a single-ended measurement with respect to ground. This is a good approximation for many types of measurements using the ADC. The time constant of the Thevenin equivalent will be the product of the resistance and capacitance shown. However, many Silicon Labs ADCs also have the ability to make differential measurements. In this case, the equivalent circuit is different as shown in the figure below. To observe how this affects settling time, we calculate the new time constant. The time constant of the new equivalent circuit is the same as in a single-ended measurement. This circuit will have a different resistance and capacitance, but the product will be the same and thus the settling time will be the same:

$$\text{differential} = 2 \times R \times \frac{C}{2} = R \times C = \tau_{\text{single}}$$

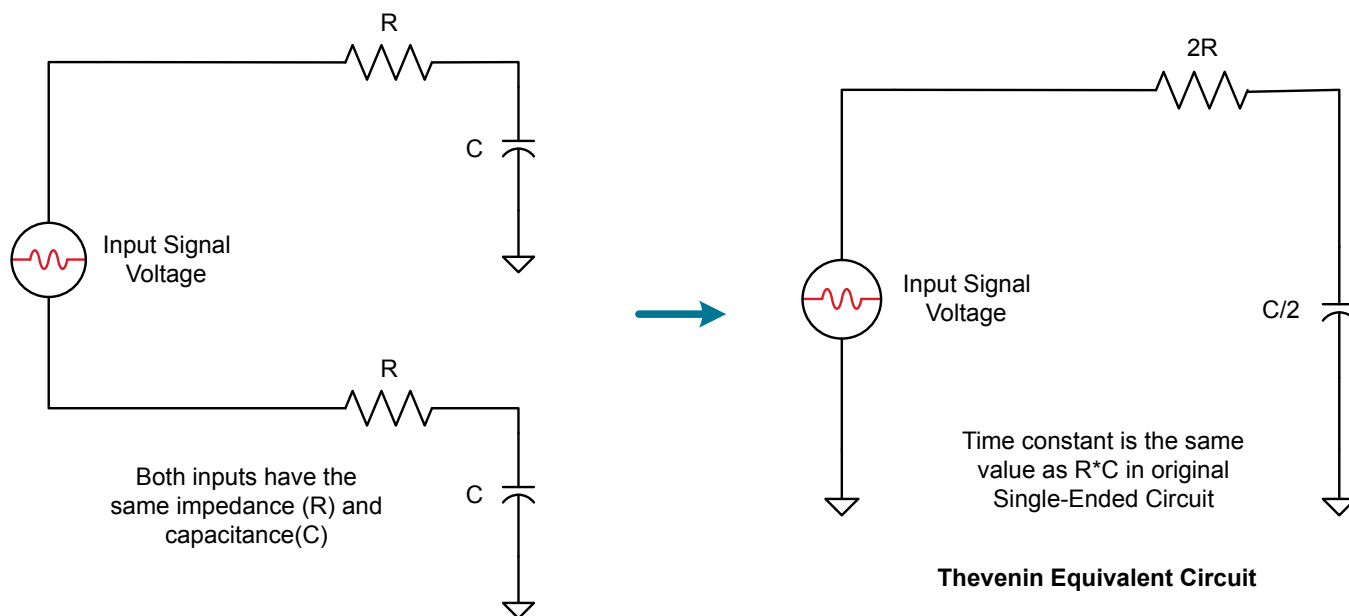


Figure 1.2. Differential Measurement Time Constant

## 2. Determining Settling Time

The settling time required for a given application is determined by the ADC input circuit, external circuitry (e.g., anti-alias filter), and the ADC settling time specification. If proper settling requirements are not met, then the ADC may not meet the specifications posted in the data sheet. One must consider the settling time of the ADC input circuit, external circuitry, and the minimum required by the ADC specification in order to calculate settling time requirements. We design to the most restrictive requirement.

### 2.1 Minimum Settling Time Specification

Silicon Lab's ADC specification requires a 1.5  $\mu\text{s}$  tracking time. Even though [Figure 1.1 Equivalent ADC Circuit for Estimating Settling Time on page 1](#) presents an equivalent circuit for settling time estimation, the actual ADC peripheral has numerous components that affect settling time such as switched capacitors, transmission gates, etc. Thus, the minimum specified settling time is 1.5  $\mu\text{s}$ . If the calculated settling time using the equivalent circuit in [Figure 1.1 Equivalent ADC Circuit for Estimating Settling Time on page 1](#) or the external circuit is greater than 1.5  $\mu\text{s}$ , then the settling time will be dictated by external components.

### 2.2 Settling Time of the ADC Input Circuit

Because the equivalent input tracking circuit of the ADC is an RC circuit, we will calculate settling time in terms of time constants. It is useful to specify settling time as the number of time constants it will take for an accuracy specified as a fraction of the least significant bit (LSB):

$$\text{LSB} = \frac{V_{\text{REF}}}{2^N}$$

To calculate the time (t) required for the sample capacitor voltage to settle to within one-fourth of an LSB of the input voltage, we derive an equation for the calculation:

$$V(t) = V_{\text{in}} \times \left(1 - e^{-\frac{t}{\tau}}\right)$$

In this equation,  $V_{\text{in}}$  is the input voltage at the input pin of the device and the time constant is  $\tau = RC$ . Solving for t in terms of the number of time constants,  $\tau$ , we obtain the result:

$$t = -\ln\left(1 - \frac{V(t)}{V_{\text{in}}}\right) \times \tau$$

To calculate the voltage to be within 1/4 LSB of the input voltage, assuming a full-scale step input ( $V_{\text{in}} = V_{\text{REF}}$ ):

$$V(t)_{\frac{1}{4}\text{LSB}} = V_{\text{REF}} \times \left(1 - \frac{1}{2^N \times 4}\right)$$

Substituting and again assuming a full-scale step input ( $V_{\text{in}} = V_{\text{REF}}$ ), we obtain the following result:

$$t = -\ln\left(\frac{1}{2^N \times 4}\right) \times \tau$$

In this equation, N is the number of ADC bits. Assuming a 12-bit ADC, this equation becomes:

$$t = -\ln\left(\frac{1}{4096 \times 4}\right) \times \tau = \ln(4096 \times 4) \times \tau = 9.7 \times \tau$$

Note that this equation is for a 12-bit ADC, where a 1/4 LSB accuracy is desired. If we are using an 8-bit ADC and also want 1/8 LSB accuracy, then this equation becomes:

$$t = \ln(256 \times 8) \times \tau = 7.6 \times \tau$$

As shown in [Figure 1.1 Equivalent ADC Circuit for Estimating Settling Time on page 1](#), we estimate the impedance and capacitance to be  $R = 5 \text{ k}\Omega$  and  $C = 10 \text{ pF}$ . Substituting the values of R and C,  $\tau = 50 \text{ ns}$ . Thus, the settling time for the 12-bit ADC and 1/4 LSB accuracy is about 500 ns, and the 8-bit ADC with 1/8 LSB accuracy is 380 ns. However, the ADC specification for minimum settling time is 1.5  $\mu\text{s}$ , which is more restrictive in both cases.

### 2.3 External Circuit Settling Time

When the external circuitry is connected to the analog input pin, the settling time may be affected. Such circuitry typically includes an anti-aliasing filter used to remove higher frequency noise that will alias or fold into the signal band of interest. There are many different filter designs, and all will affect input impedance and have a settling time associated with them. The external circuit's capacitance and output impedance will affect the settling time. The design of anti-alias filters should be designed to drive the approximately 10 pF in the ADC input circuit. Such effects must be considered when calculating settling time of the ADC measurement. If the input filter settling time is extremely long, then this settling time will dictate the settling time of the system.

## 2.4 External Circuit Examples

### Passive RC Anti-Aliasing Filter

These low-pass filters use passive components (resistors and capacitors). A single-pole passive filter will have a higher impedance and longer settling time. However, if the filter's capacitor is an order of magnitude higher than the sample capacitor, the filter capacitor will charge the sample capacitor quickly. Thus, once the filter settle time is satisfied, the application then switches to that input, and the filter capacitor can charge the sample capacitor within the internal ADC circuit specification time (1.5  $\mu$ s).

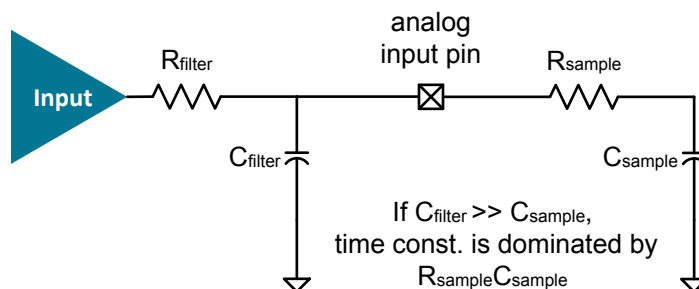


Figure 2.1. Passive Anti-Aliasing Filter

### Active Anti-Aliasing Filter

These filters utilize operational amplifiers (op-amps) in combination with resistors and capacitors to implement low-pass filters. These filters form good buffer stages as they have higher input impedance and lower output impedance. Op-amps may introduce some noise. Refer to the manufacturer's data sheet for such information when considering design of filters with op-amps.

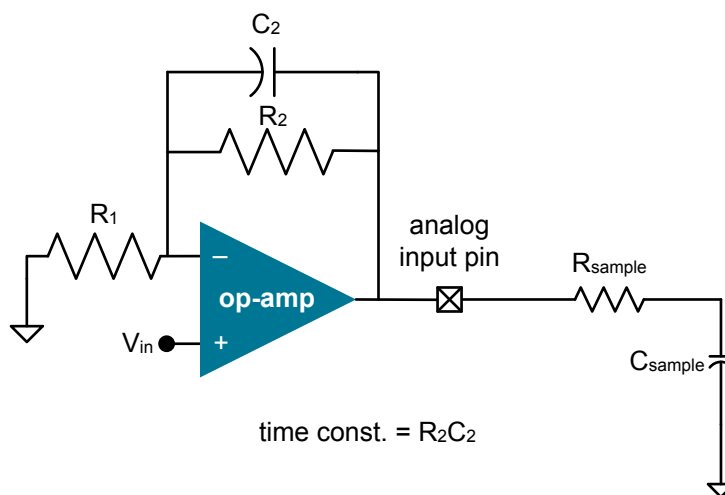
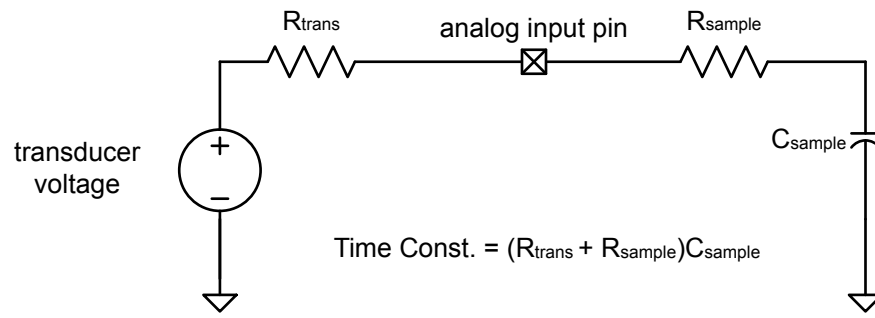


Figure 2.2. Active Anti-Alias Filter

### Measurement Transducer Circuit

Transducers provide a measurement voltage that is proportional to a measured parameter (e.g., pressure or weight). Such devices are typically high impedance circuits represented by a voltage source and a large resistance. In this case, the settling time is dictated by the transducer's impedance.



**Figure 2.3. Transducer Circuit Equivalent**

### 3. Methods For Satisfying Settling Time Specification

There are various methods for handling settling time requirements of both the tracking circuit and external circuitry. The best way to avoid settling time errors will depend on the specific application.

#### 3.1 Low-Power Tracking Mode

Low-power or delayed tracking mode is a useful method to ensure the minimum settling time requirement is satisfied. When a conversion is initiated while in this tracking mode, the device automatically tracks for a number of SAR clock cycles before performing the data conversion. This tracking time is calculated to meet the minimum input tracking time of the ADC. The tracking mode timing diagrams in [Figure 3.1 Low Power or Delayed Tracking Timing Diagram with External Conversion Start on page 7](#) and [Figure 3.2 Low Power or Delayed Tracking Timing Diagram with Internal Conversion Start on page 7](#) show the tracking and conversion timing with respect to the SAR clock and trigger source that initiates the track/convert process.

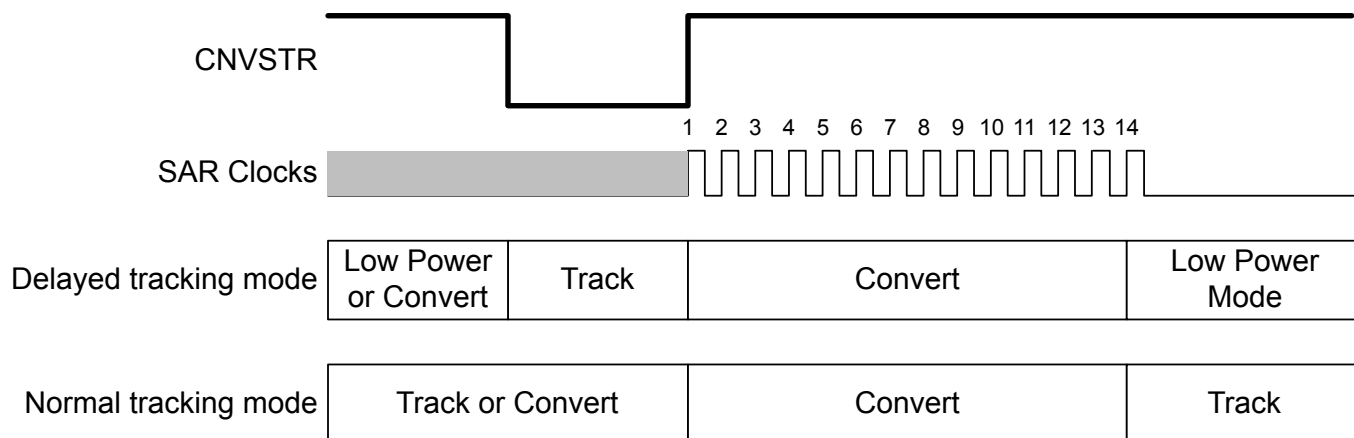


Figure 3.1. Low Power or Delayed Tracking Timing Diagram with External Conversion Start

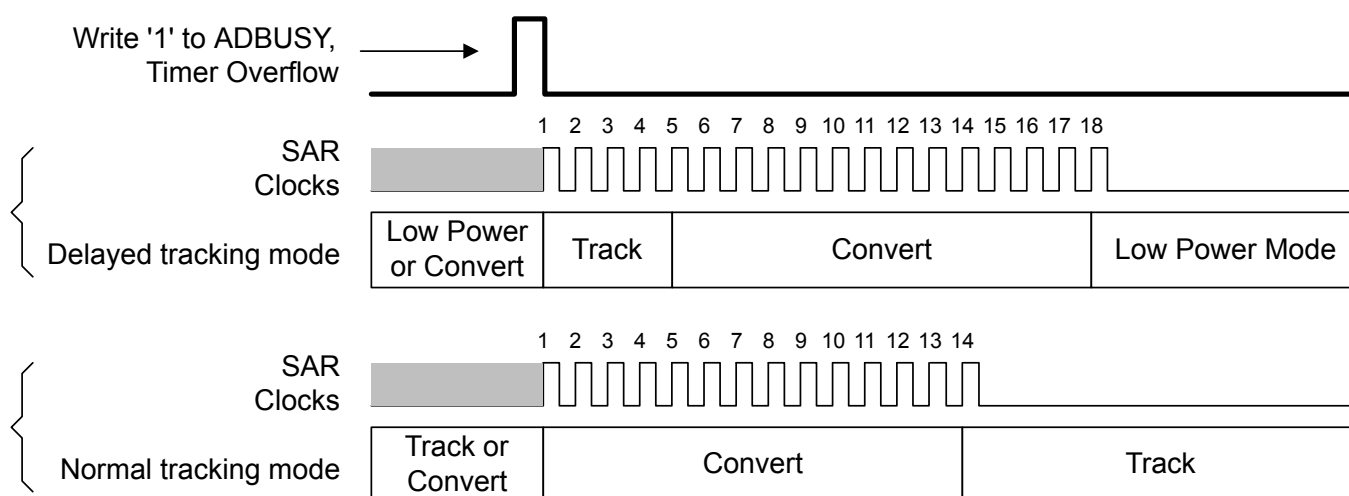


Figure 3.2. Low Power or Delayed Tracking Timing Diagram with Internal Conversion Start



### 3.2 Manually Controlling Settling Time

Once the AMUX is set to sample an input pin, the tracking circuit will begin to charge the sample capacitor. The external input circuit should be designed to drive 10 pF in the tracking circuit, ideally within the minimum 1.5 μs settling time. If low power or delayed tracking mode is not used, the ADC will track the input continuously and a start of conversion signal will initiate an immediate data conversion. The user must calculate proper settling time and initiate a conversion via an internal signal (i.e., a Timer) or an external signal (CNVSTR).

### 3.3 Multiple ADC Inputs

Many applications will use the ADC to measure parameters from several sources by switching the ADC input analog multiplexer. This is a useful technique, but the settling time specifications must be considered when switching the analog multiplexer settings (i.e., changing the input to the ADC). Each time the application software switches from one ADC input to another, there must be at least 1.5 μs of settling time prior to initiating an ADC conversion.

**Note:** Switching the input channel and initiating a data conversion without waiting for the appropriate settling time can give the appearance of sampling the previous input channel. This is because the sampling capacitor will still hold approximately the same charge from the last data conversion.

We recommend placing the ADC in low power tracking mode and initiating ADC conversions after the AMUX settings have been switched. In this way, the ADC will track for some SAR clock cycles before an ADC conversion but after the ADC input was changed by the analog multiplexer.

### 3.4 Low Power Applications

If the designer wishes to use a power saving mode (e.g., Idle mode), it is recommended that low power or delayed tracking mode be used to ensure the minimum settling time requirement is met upon waking the device. The MCU is placed in a power saving mode between samples. After an ADC data conversion is complete, the device is placed back into Normal mode, and the ADC sample is processed and stored. If the application polls the ADBUSY bit, then the MCU will have to be in Normal mode during the data conversion, as well. The ADC will then track for some SAR clock cycles and then perform the data conversion. After the sample is processed, the device can then be placed back into a power saving mode. Thus, low power tracking can be used to ensure the minimum settling time requirements are satisfied when using the ADC in low power applications (i.e., waking the device from Idle mode only for sample processing).

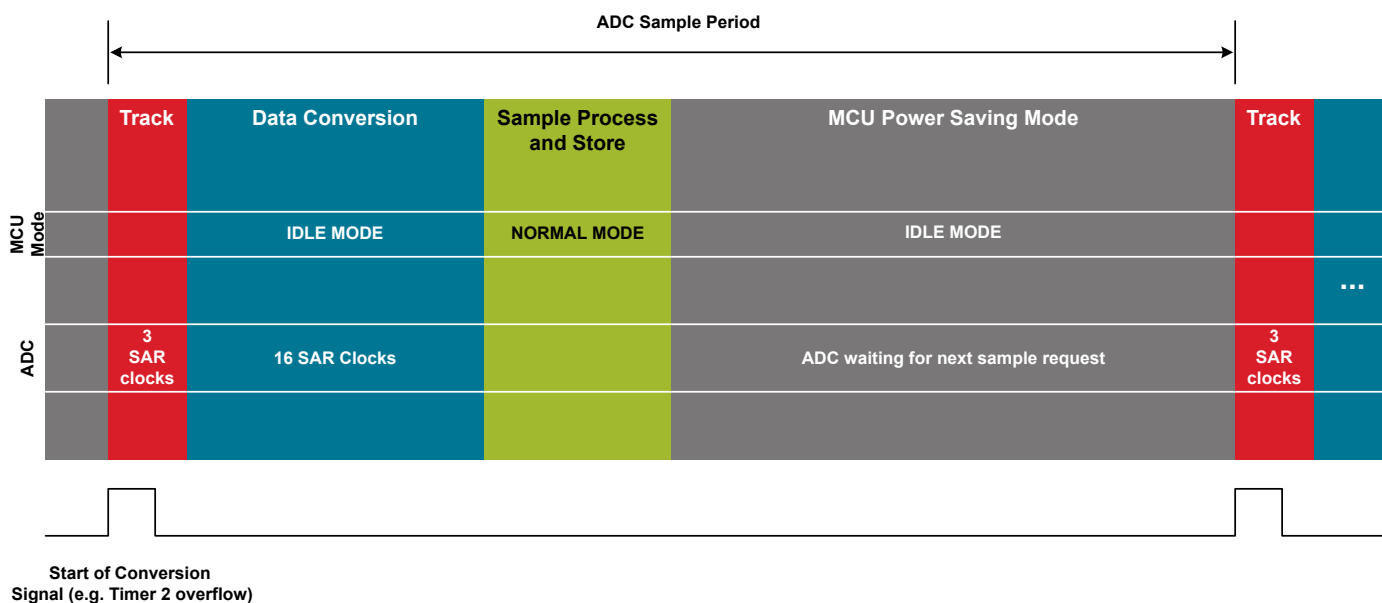


Figure 3.3. Delayed Tracking Mode used with Power Saving Mode

Additionally, settling time of the external circuitry can be satisfied while the device is in a power saving mode. For example, the input signal can be allowed to settle in an anti-aliasing filter while in a power saving mode. Once this settling time has passed, the signal to wake the device and initiate a track and conversion is sent such that the device is in lower power mode for as long as possible, and the 1.5 μs settling time specification will be met with the external circuit settling time already satisfied.

### 3.5 Temperature Sensor

The internal temperature sensor on some devices can require additional settling time. If the temperature sensor measurement doesn't match expectations, it is recommended to increase the time between conversions until the temperature sensor measurement is as expected. Then, decrease the delay iteratively until the minimum settling time is reached.

## 4. Summary

Settling time must be considered in designs that utilize the ADC for measurements. If settling time requirements are not met, the ADC measurements may not meet posted specifications.

The settling time requirement of a system may be affected by the external circuitry (time constant and output impedance), ADC input circuit, and the ADC settling time specification posted in the data sheet (1.5  $\mu$ s).

A Thevenin equivalent circuit of the ADC input and external circuitry should be used to estimate the most conservative settling time requirement. If this settling time requirement is less than the 1.5  $\mu$ s ADC specification, then the 1.5  $\mu$ s specification should be used.

[Table 4.1 Satisfying Settling Time on page 10](#) summarizes the guidelines when determining which method will be best to satisfy the system's settling time requirements.

**Note:** 1.5  $\mu$ s settling time may not be the most restrictive settling time requirement.

**Table 4.1. Satisfying Settling Time**

ADC Sample Technique	How Accomplished	Comments
Manual	Software delay	More control for the designer, but must ensure that the ADC settling time specification of 1.5 $\mu$ s is met.
Delayed tracking mode	Set the appropriate field in the ADC0CN0 register	Automatically tracks for some number of SAR clocks prior to performing data conversion. Enforces the 1.5 $\mu$ s settling time specification upon start of conversion signal.
Multiple ADC inputs	Use the analog multiplexer to switch the ADC input in firmware	Recommend using low-power tracking mode. When the analog multiplexer setting is changed, initiate conversion and ADC will track for some number of SAR clocks prior to data conversion. <b>Note:</b> Tracking of at least 1.5 $\mu$ s is required each time ADC input is changed!
Low power applications	Use delayed tracking mode, disable the ADC when not in use, and use the MCU power-saving modes	Use low power or delayed tracking mode to ensure 1.5 $\mu$ s settling time specification is met when waking device from Idle mode between samples. Delayed tracking saves some power compared to continuously tracking, but it is best to disable the ADC when not in use.
Internal temperature sensor	Add extra settling time, as needed	Reduce the rate of the conversion start source until the temperature sensor measurements meet expectations. Then, iteratively increase the rate of conversions until the minimum settling time is found.



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