8/16/32-Bit

A Guide to the Analog Part of the A/D Converter

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Device1
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1 Introduction

The majority of Infineon Microcontroller products include an integrated, on-chip A/D (Analog/Digital) converter for analog signal measurement, with multiplexed input channels and a sample and hold circuit.

Depending on the device type, the integrated A/D converter allows resolutions of 8-bit, 10-bit or 12-bit. Because the A/D converter uses the Successive Approximation (SAR) method, it is also known as the SAR-A/D converter (Successive Approximation Register A/D converter). This A/D converter type uses binary weighted conversion capacitors and one sample and hold unit per A/D converter.
Other types of A/D converter with non binary weighted conversion capacitors, such as FADC (Fast A/D converter) or with multiple sample and hold units per A/D converter are not covered in this Application Note. The DS-A/D converter (Delta Sigma A/D converter) is also not covered in this Application Note.

In principle, the A/D converter can be divided into two parts:

- Analog part
  - including the converter with sample and hold circuit
- Digital part
  - which contains registers and the digital control unit

This Application Note provides basic information and recommendations for the analog part of the A/D converter. Please refer to the appropriate microcontroller User Manual for the description of the digital part.

For historical and evolutionary reasons, different implementations of the A/D converter are available. The differences in the analog part mainly concern the values in the A/D converter characteristics specified in the related Data Sheet.

The resolution (r) of the A/D converter refers to the number of quantization levels an analog input voltage can be determined to. The number of smallest levels is given in bits and one of these is the Least Significant Bit (LSB). **Figure 1** shows an example of an A/D converter with 2^{10} - 1 = 1023 output quantization levels.

An A/D converter with 10-bit resolution quantizises an analog input voltage of 5 V to a step size of:

5 V / 2^{10} = 4,88 mV

The values represent the digital output range from 0 to 1023.

This theoretical accuracy of an A/D converter is degraded by inaccuracies of the A/D converter itself (total unadjusted error). Additionally the accuracy of the complete A/D conversion system is degraded by the external elements which are connected to the analog input ANx and to the reference voltage V_{AREF}. It is the task of the system designer to keep the inaccuracies caused by the external circuits as low as possible, and this Application Note provides the necessary basic information to optimize the external circuits of the A/D converter.

2 Transfer Characteristic and Error Definition

The following diagrams show the ideal transfer characteristic of an A/D converter and the definitions for the different kinds of error specified in the related Data Sheet:

- Offset Error
- Gain Error
- Differential Non-Linearity Error (DNLE)
- Integral Non-Linearity Error (INLE)
- Total Unadjusted Error (TUE)

2.1 Ideal Transfer Characteristic

Figure 1 defines the ideal transfer characteristic for an A/D converter.

The Ideal Transfer Curve (1) transfers each input to an output.

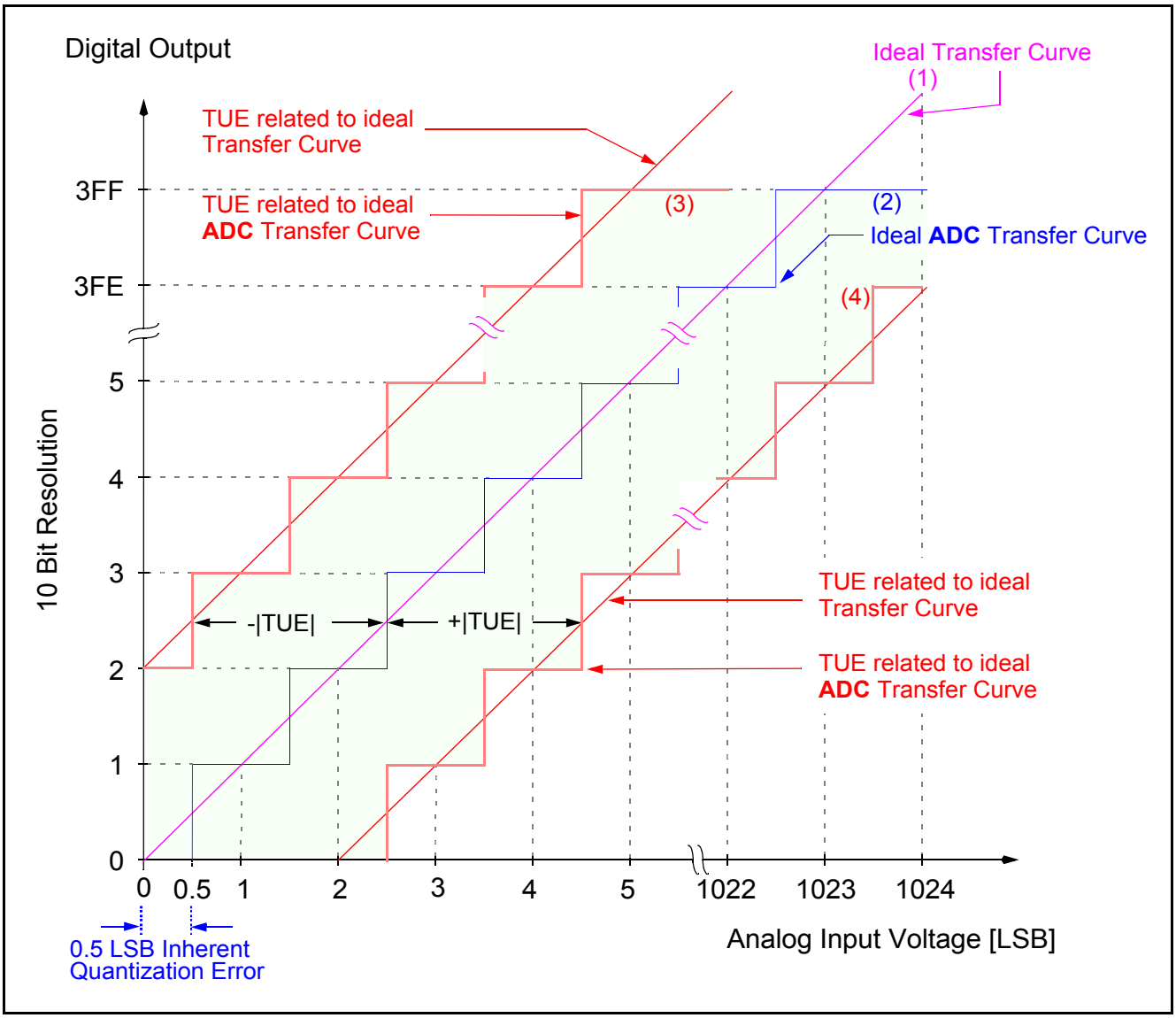

Figure 1 Ideal Transfer Characteristic

The Ideal ADC Transfer Curve (2) includes a quantization error, since all analog input values are presumed to exist, they must be quantized by partitioning the continuum into discrete digital values. All analog values within a

given range (quantization step) are represented by the same digital value, which corresponds to the nominal mid-range value. That is the reason for the quantization uncertainty of +/- 0.5 LSB, which is a natural error and inherent to each A/D converter.

The analog input voltage range must be within V_{AGND} up to V_{AREF}.

The quantization step size is 1 LSB = V_{AREF} / 2^r.

According to the Ideal Transfer Curve (1) the first digital transition, from 0 to 1, is shifted to the analog value of 0.5 LSB to get a minimum quantization uncertainty. That is why the first step width of the Ideal ADC Transfer Curve (2) is 0.5 LSB, and the last step width is 1.5 LSB with an digital output range from 0 to (2^r - 1).

The compensated inherent quantization error in relation to the analog input voltage is shown in **Figure 2**.

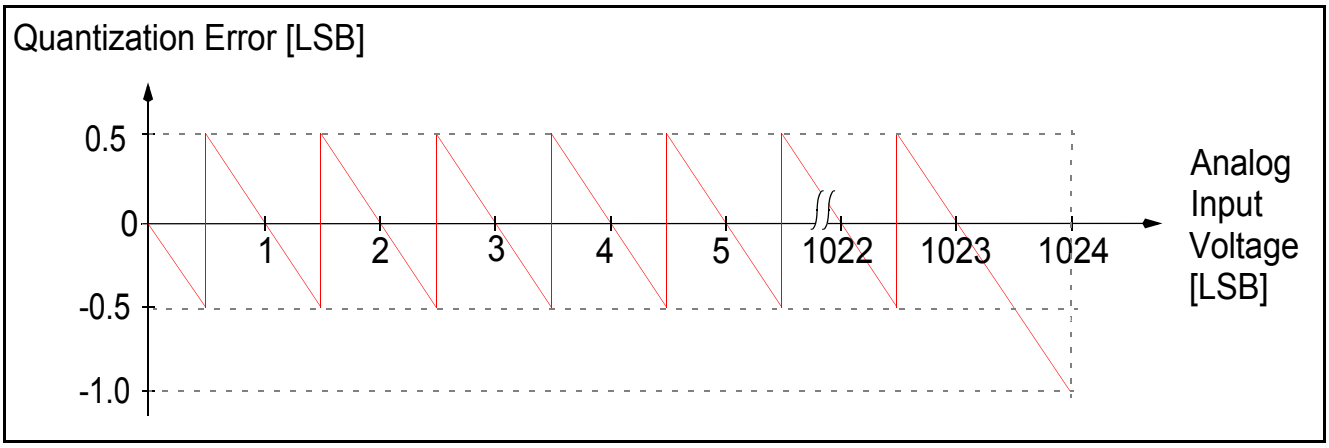

Figure 2 Quantization Error

The total unadjusted error includes all A/D converter related inaccuracies such as production process deviations and internal noise.

The TUE consists of offset error, gain error, DNLE and INLE, but it is not simply the sum of individually measured errors. Because some ADC errors such as offset and gain, can compensate each other, the TUE can be far less than the absolute sum of all individual errors. **Figure 1** shows the definition of the TUE in relation to the Ideal ADC Transfer Curve (1).

The real result of the A/D converter is in the range of Ideal ADC Transfer Curve (2) +/- TUE. This area is shaded in **Figure 1** and is between both TUE related to ideal ADC Transfer Curves (3) and (4).

Note: Reference voltages are considered as the ideal. An incorrect reference voltage generates an additional error.

2.2 Offset Error

The offset error is the deviation from the Ideal ADC Transfer Curve at the lowest transition level on the Real ADC Transfer Curve. It is the input voltage required to bring the digital output to zero and can be measured by determining the first digital transition, from 0 to 1, of the A/D converter. The offset error affects all codes by the same amount.

In the following figure all other kinds of error (gain, DNLE, INLE) are excluded.

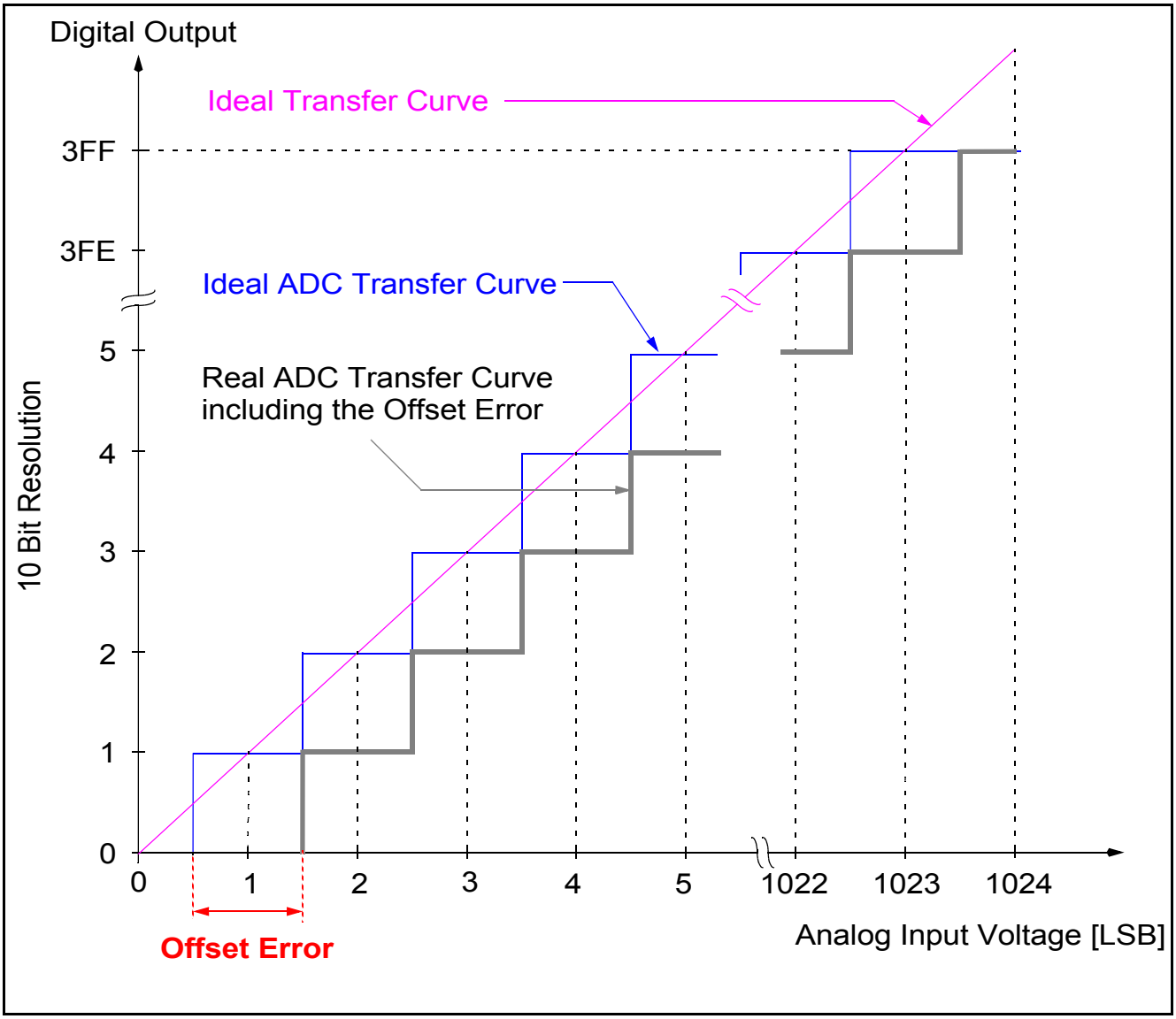

Figure 3 Offset Error

2.3 Gain Error

The gain error is the difference between the slopes of the real ADC Transfer Curve and the Ideal ADC Transfer Curve at the maximum digital out value.

In the following figure all other kinds of error (offset, DNLE, INLE) are excluded.

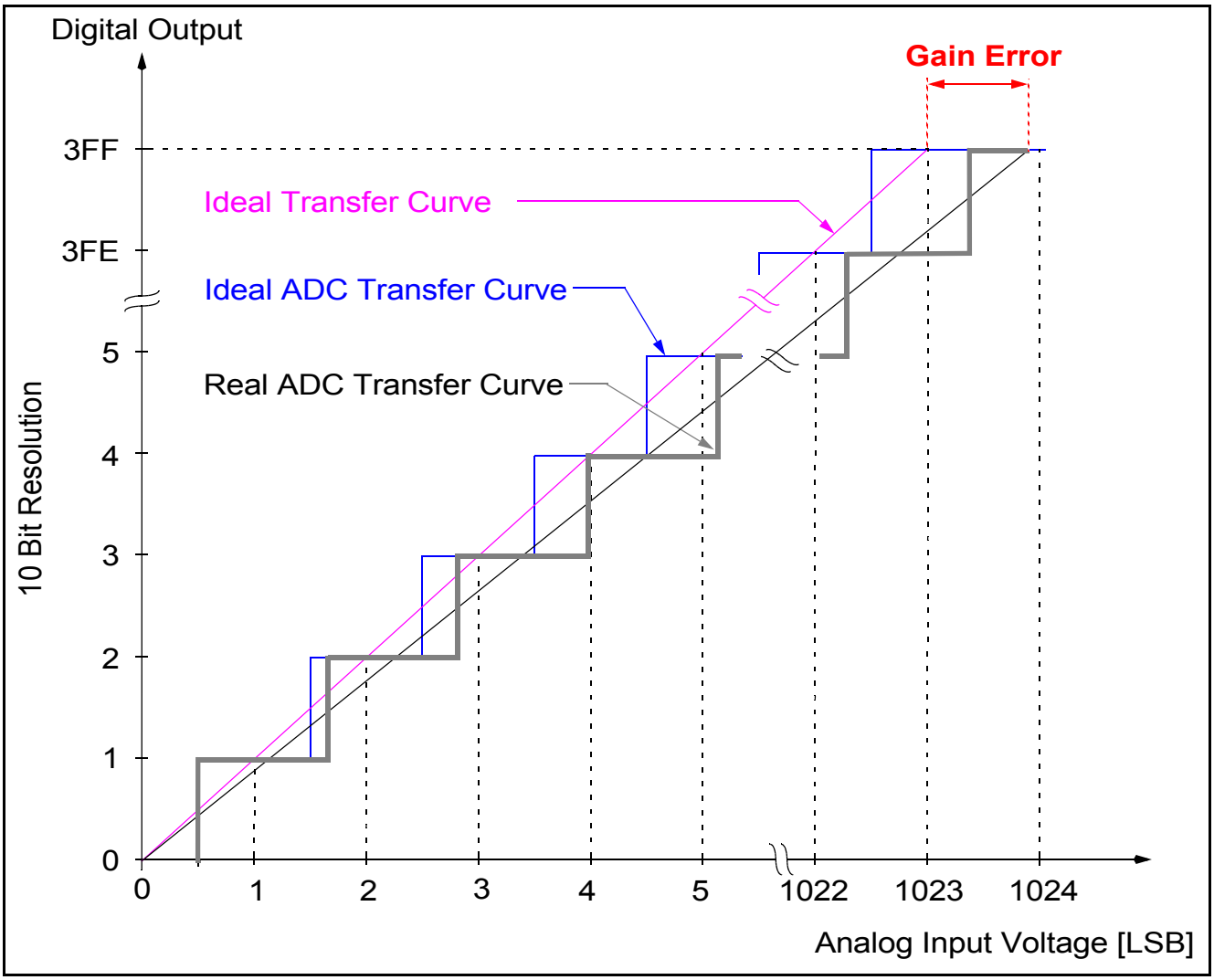

Figure 4 Gain Error

2.4 Differential Non-Linearity Error (DNLE)

The DNLE describes variations in the analog value between adjacent pairs of digital numbers, over the full range of the digital output.

If each transition step width is exactly 1 LSB, the DNLE is zero.

If the transitions are 1 LSB +/- 1 LSB, then there is the possibility of missing codes. If a missing code occurs then one value of the digital output is missing; e.g. the digital output might jump from 0011 to 0101 and miss out 0100 (See the figure that follows).

If the DNLE is less than 1 LSB, then a missing code is automatically excluded. In the following figure all other kinds of error (offset, gain, INLE) are excluded.

If the output code always increases with an increase of the analog input and always decreases with a decrease of the analog input, then the A/D converter is monotonic. The A/D converter is called monotonic when the DNLE is in the range of -1 LSB ≤ DNL ≤ 1 LSB.

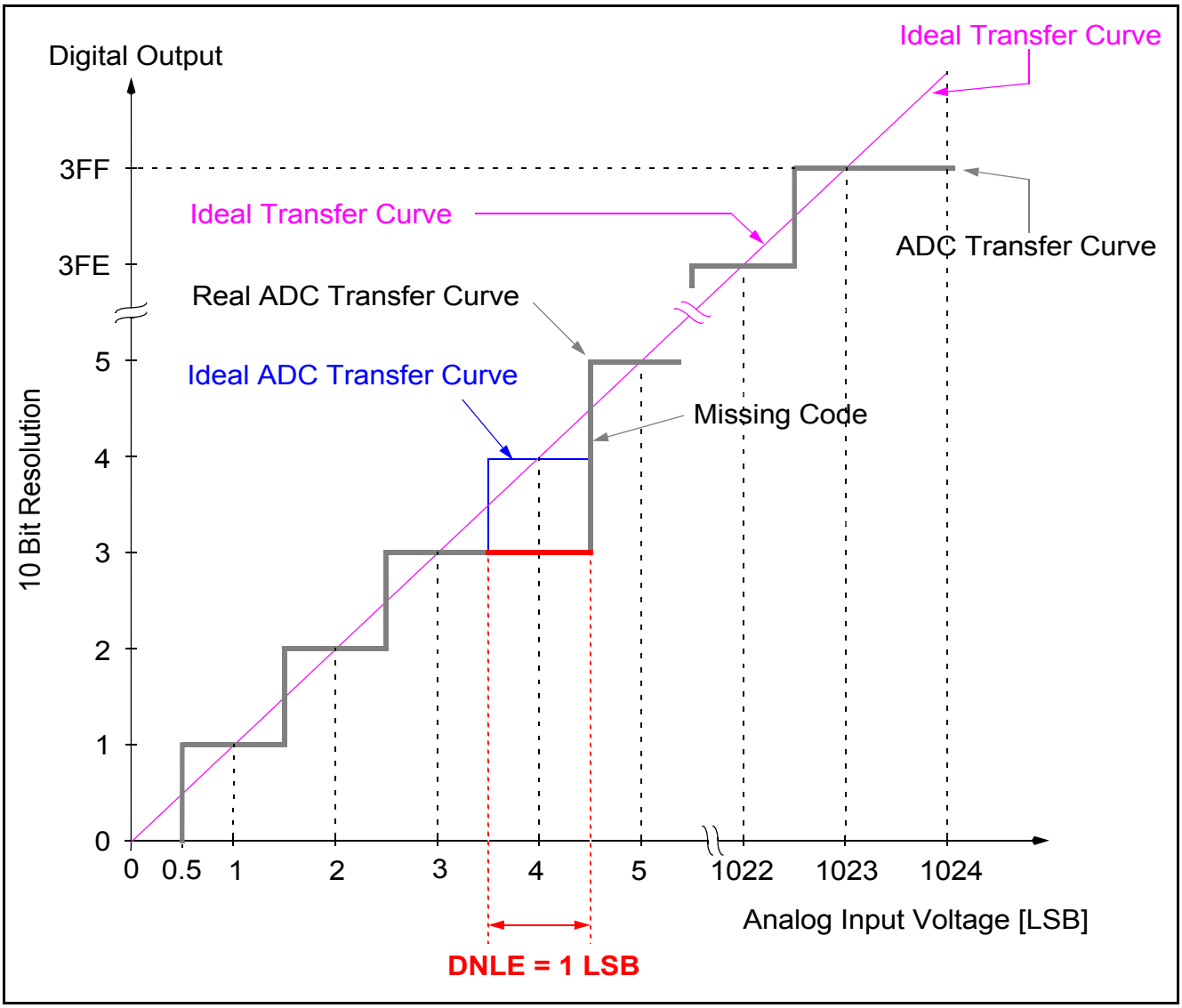

Figure 5 Differential Non-Linearity Error

2.5 Integral Non-Linearity Error (INLE)

The INLE is the maximum difference between the Ideal ADC Transfer Curve and the adjusted Real ADC Transfer Curve (without offset and gain error). In the following figure DNLE is also excluded.

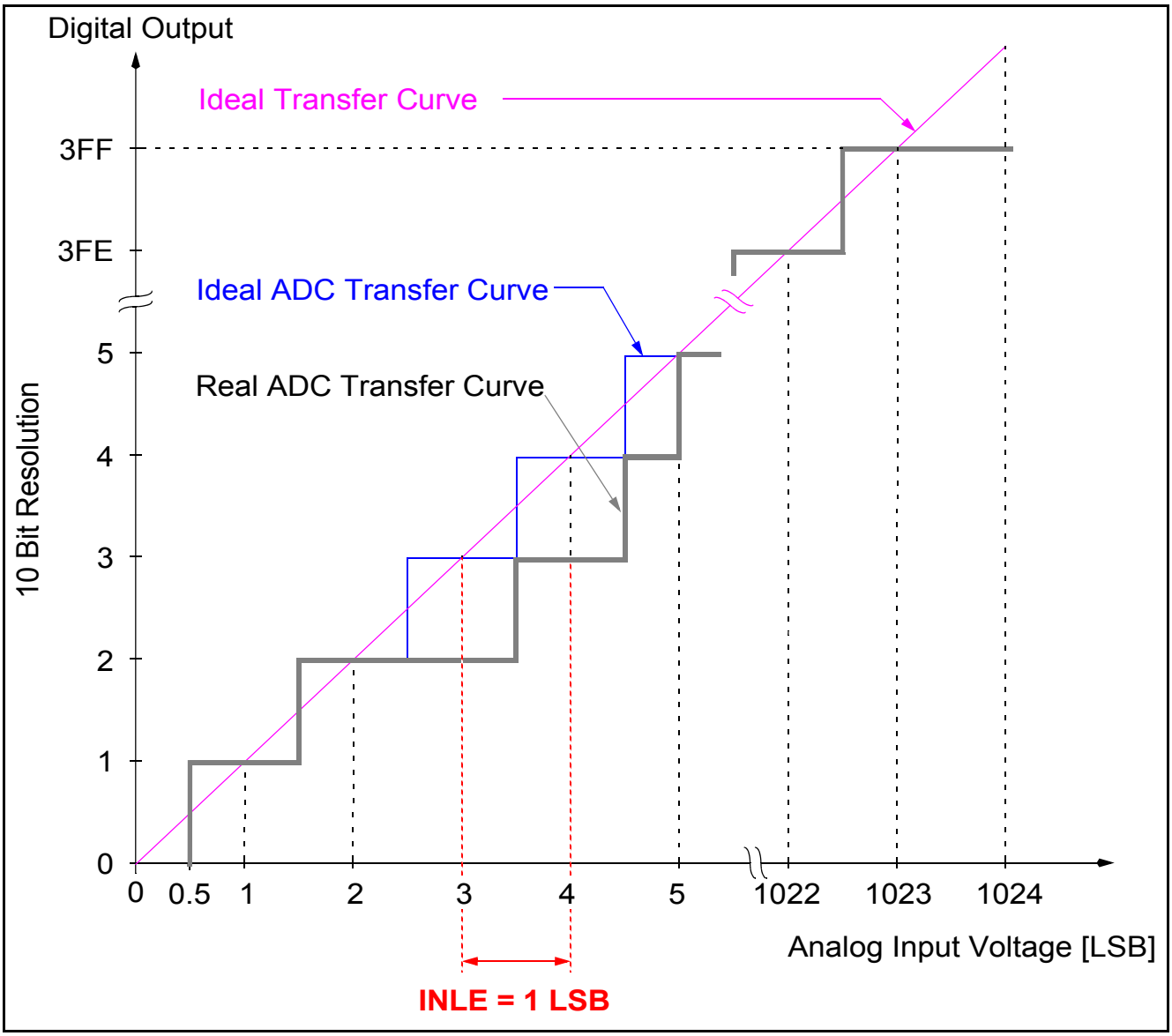

Figure 6 Integral Non-Linearity Error

3 Principle of Conversion

The A/D converter is based on the principle of Successive Approximation. It uses a capacitor network in order to compare the analog input voltage with a reference voltage, generated from V_{AREF} and V_{AGND}. This reference voltage is adapted step by step through Successive Approximation.

The capacitor network is also used for the sample and hold function. The conversion is performed in several steps. A total conversion consists of:

- Sample phase
- Charge-redistribution phase (conversion phase)
- Calibration phase (only A/D converter with enabled calibration)
- Write-back phase

The sequence of the different phases is shown in **Figure 7**. The total ADC conversion time is controlled via software. The block diagram in **Figure 8** is related to a calibrated A/D converter with 10-bit resolution and represents the principle connections between the analog input ANx, conversion C-net, comparator, and the A/D converter result register.

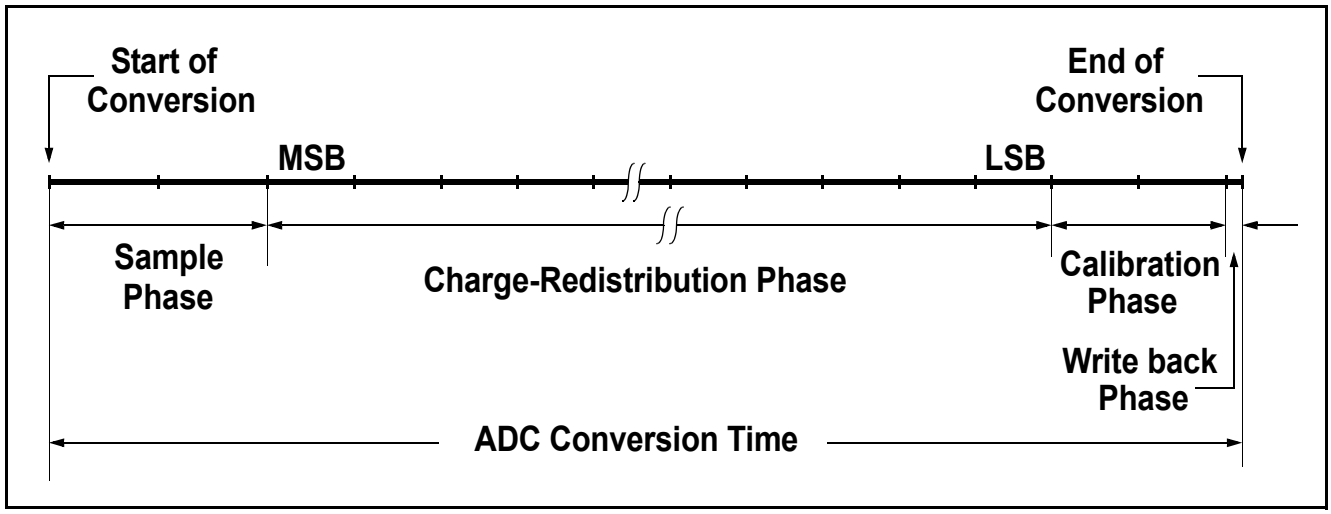

Figure 7 A/D Converter Timing

3.1 Sample Phase

During the sample phase, the conversion control unit connects the capacitors of the conversion C-net to one of the analog input channels via a multiplexer. The capacitor network is therefore charged/discharged to the voltage level of the connected analog input channel. The hold capacitor C_{HOLD} at the comparator holds the analog input voltage after the sample phase.

3.2 Charge-Redistribution Phase

At the end of the sample phase and with the start of the charge-redistribution phase, the conversion C-net is disconnected from the analog input. Now the voltage level stored in the hold capacitor C_{HOLD} is reconstructed by connecting the C-net capacitors C_{r-1} to C_0 (r: A/D converter resolution) individually to V_{AREF} or V_{AGND}.

As the capacitor network (conversion C-net) is binary weighted (i.e. $C_n = 2*C_{n-1}$), the charge of the capacitors C_{r-1} to C_0, corresponds directly to the voltage level of the connected analog input channel. The digital value is found successively, starting from the most significant bit down to the least significant bit. The comparator is used to decide whether the actual voltage of the capacitor C_n is below or above the voltage stored in the hold capacitance.

The charge-redistribution phase is finished after ‘r’ steps of successive approximation, with r: 8, 10 or 12.

3.3 Calibration Phase

Note that only an A/D converter with calibration features can perform a calibration phase.

The conversion accuracy depends on the precision of the conversion C-net and the offset voltage of the comparator. In order to correct the errors that are introduced through process variations and offset voltage, an additional C-net (the calibration C-net) is used together with calibration control logic. A detailed description of the calibration phase is in **Chapter 4 "Calibration Mechanism (Error Correction)" on Page 15**.

3.4 Write-Back Phase

During the write-back phase, the result of the Successive Approximation is copied to the A/D converter result register and the conversion C-net is pre-charged with approximately V_{AREF} / 2.

Note: Because of parasitic capacitances caused by the pads and the analog multiplexer, the pre-charge voltage at the pins can differ from V_{AREF} / 2, but is typically less than V_{AREF} / 2.

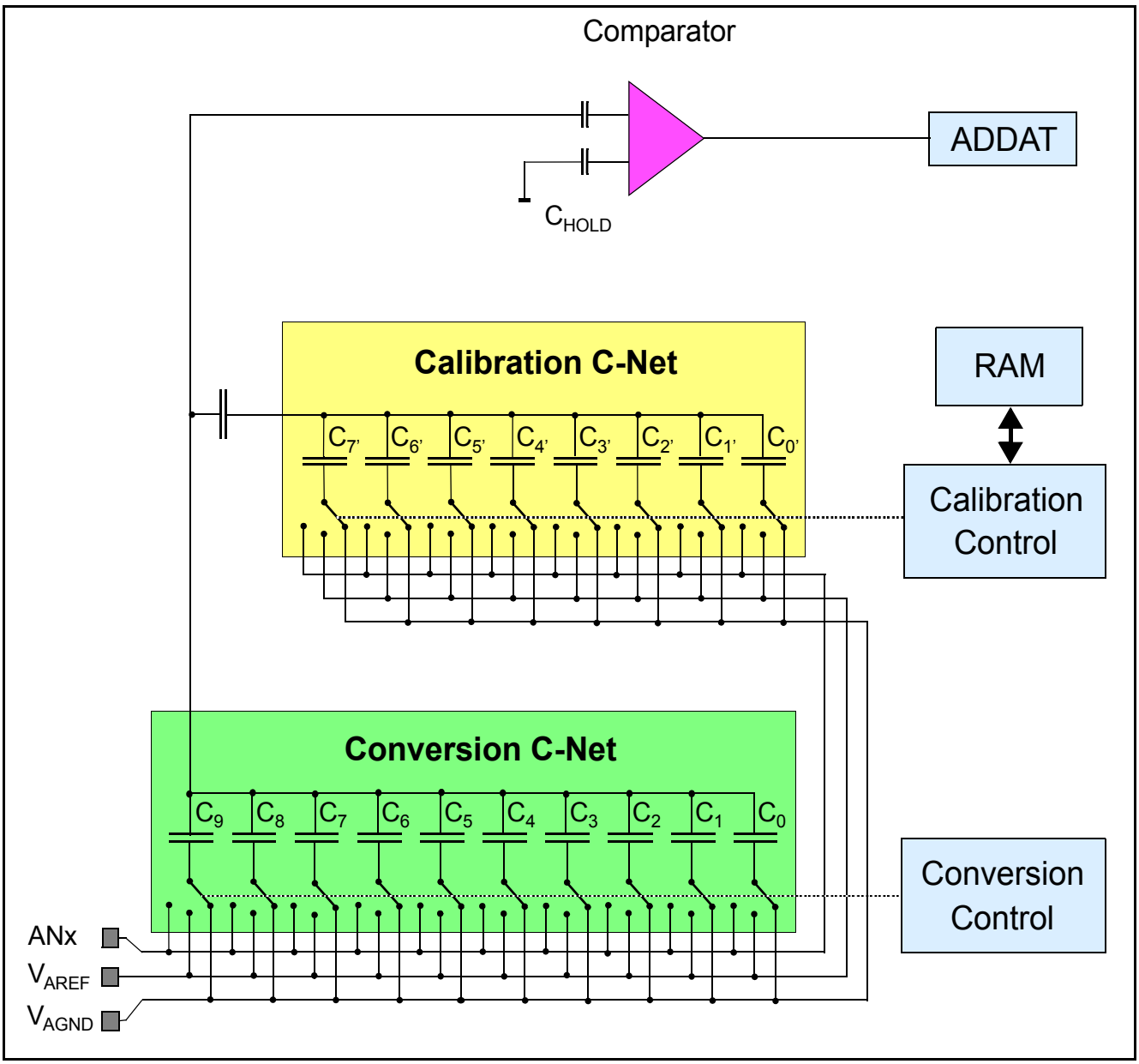

Figure 8 Block Diagram: Analog Part of a 10-bit A/D Converter with Calibration and Conversion C-Nets

4 Calibration Mechanism (Error Correction)

The self-calibration mechanism is implemented in the A/D-converter in order to compensate for the offset error and to balance differences in the capacitive network due to production variations, which can cause linearity deviations of the A/D conversion.

Note: Because of different demands for accuracy, die size or conversion time restrictions, not all SAR-A/D converters provide the calibration feature.

The self-calibration mechanism consists of the:

- Calibration capacitor-net
- Calibration RAM
- Calibration control unit

*Note: For a block diagram, see **Figure 8**.*

Self-calibration includes two different kinds of calibration:

- Offset Calibration
  - The adjustment of the offset error
- Linearity Calibration
  - The binary weight adjustment between the capacitors of the conversion capacitor-net

4.1 Calibration Principle

The additional correction capacitor-net (calibration C-net) is used to add/subtract a capacitive charge to the comparator input of the A/D converter. A typical implementation of the correction C-net allows an adjustment in the range of ± 4 LSB with a resolution of 1/32 LSB within ± 128 steps.

The same calibration C-net is used for both the offset and the linearity calibrations:

- During offset calibration the corrective charge is determined, in order to zero-adjust the comparator.
- During linearity calibration, for each of the binary weighted capacitors of the conversion C-net, a correction value (with respect to the sum of the remaining capacitors) is determined.

The results of the calibration are stored in the calibration RAM. During normal conversion, the stored values are used to correct the measurement by using the calibration control unit to calculate the appropriate combination of the calibration capacitors.

4.2 Reset Calibration

After a reset, the calibration RAM is cleared and the A/D converter automatically starts an initial full calibration sequence (power-up calibration). Both the offset and the linearity deviations are adjusted. The first quarter of this calibration sequence typically performs a coarse adjustment which becomes more precise during the remaining three quarters of the sequence. This scheme guarantees a very fast reduction of the offset and linearity error.

Notes

1. *After reset, the positive and negative analog reference voltages (V_{AREF} and V_{AGND}) must be stable and within the specified range, in order to perform a valid reset calibration.*
2. *The reset calibration can be interrupted by any conversion. If interrupted, the reset calibration is lengthened by the conversion time. The calibration sequence is performed with the actual values of the control register. A change of the Conversion Time Control also changes the duration of the calibration sequence.*
   During the reset calibration sequence, conversion results can exceed the specified maximum TUE.
3. *When entering IDLE or Slow Down Mode the reset calibration will continue until it is finished but the Power Down current increases. It is therefore recommended to wait until reset calibration is finished before entering IDLE or Slow Down Mode.*

4.3 Normal Calibration

With post-calibration enabled during A/D converter operation, a re-calibration is performed after each conversion in order to adapt to changing operating conditions such as temperature. This re-calibration is performed in single steps, where a typical calibration step is about ± 1/32 LSB.

4.4 Disturbance Filtering

Because of the way in which the calibration operation is implemented, disturbances can be filtered during the calibration.

Noise on V_{AREF} or V_{AGND} can disturb calibration for example, but instead of performing a full correction of a detected deviation (either offset or linearity) in one cycle, the calibration circuit performs a step-by-step reduction of the deviation. Therefore if during one calibration cycle a deviation caused by a disturbance is detected, the last correction value will only be incremented or decremented by one calibration step (typically 1/32 LSB).

As an example, if the disturbance would cause an offset deviation of 1 LSB, then 32 calibration steps would be necessary to correct the error. If, however, a deviation occurs during one calibration cycle but does not appear during the next calibration cycle, the previous change of the correction value will be cancelled. In other words, an incorrect calibration caused by disturbances can only occur if the disturbance lasts for a long time. Disturbances occurring during the reset calibration will be eliminated due to the long calibration sequence and post-calibration after each conversion.

5 Analog Input Circuitry Calculation (AN0 ... ANy)

Any application where an analog voltage has to be measured needs an accurate calculation of the external circuit elements involved. This is fundamental to ensure sufficient charging of the A/D converter input capacitance C_{AINSW} to the same voltage as the analog source, during the sample time. Insufficient charging of C_{AINSW} causes additional inaccuracy ($Error_{ANx}$) to the TUE of the A/D converter.

This chapter explains how to calculate the external circuits for the analog inputs. The derivation of the necessary formulas is followed by calculation examples.

Because of the different phases of a total conversion (sample and charge-redistribution time) the calculation examples are shared into different electrical models which fit best to the values of the external circuits used.

The basis for the calculations is the voltage waveform of analog input ANx, which can be observed during a conversion.

*Note: A detailed solution of the calculation without a simplified electrical model leads to at least a 2nd order differential equation. This is not covered by this document, but a more detailed description of the behavior of the A/D converter circuitry is described in "**Chapter 6 "Analog Input Circuitry Simulation (AN0 ... ANy)" on Page 34**"*

5.1 Electrical Model of the A/D Converter Input

Figure 9 is a simplified block diagram of the A/D converter showing only the elements necessary for a calculation of the external circuits.

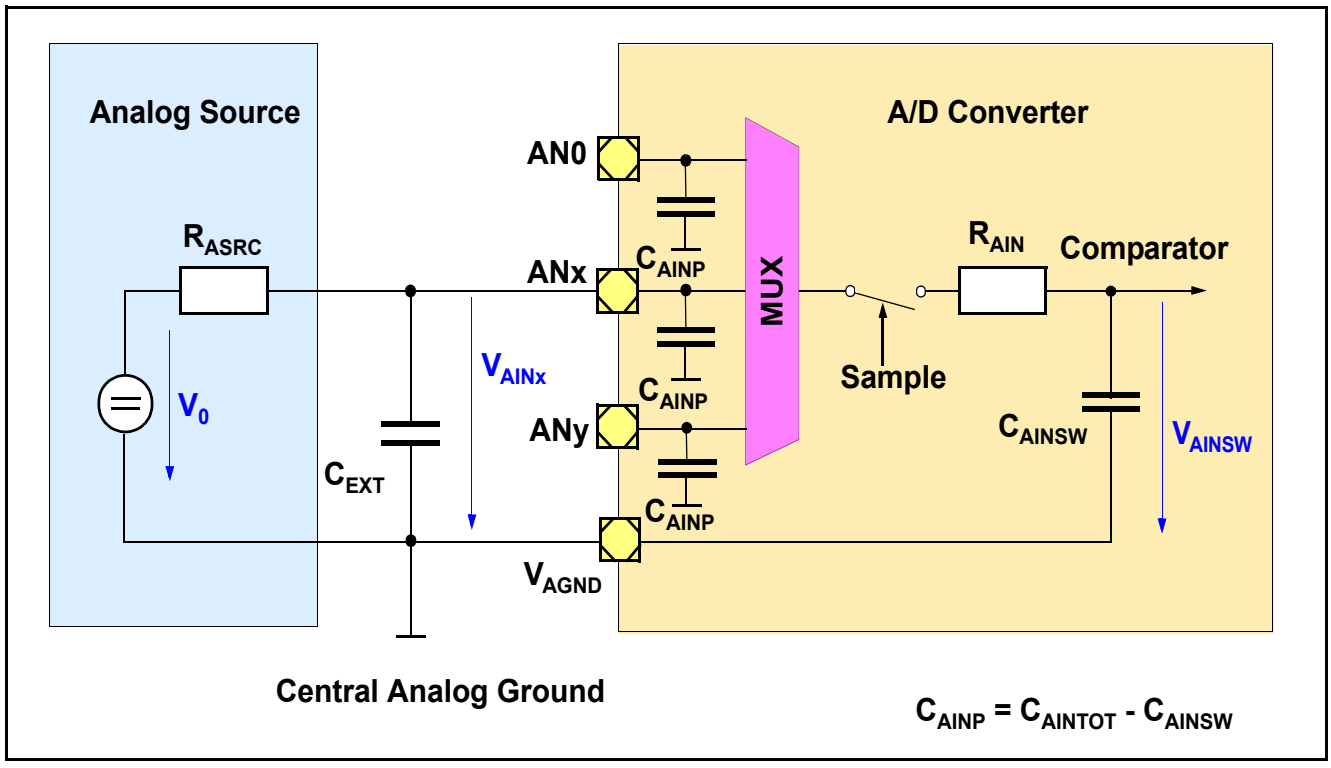

Figure 9 Block Diagram: A/D Converter Input and Analog Source

The A/D converter input capacitance C_{AINSW} contains the capacitors of the conversion C-net and all parasitic capacitors which are also switched with the sample switch.

R_{AIN} is the internal series resistance of the A/D converter.

The sample switch represents an analog switch closed only during sample time.

The multiplexer connects the selected analog input ANx with the internal conversion C-net.

The external capacitance C_{EXT} can be a real external capacitor for noise reduction, or only the parasitic capacitance caused by the signal line between analog source and A/D converter input.

The analog voltage source is represented by an ideal voltage source V_0 and a series resistance R_{ASRC}.

The specified values of R_{AIN}, C_{AINSW} and C_{AINTOT} are dependent on technology and the type of A/D converter implementation. The order of magnitude for the values is:

- C_{AINSW} ~ 20 pF
- C_{AINTOT} ~ 30 pF
- R_{AIN} ~ 1000 Ω

Note: Please refer to the Data Sheet chapter "Electrical Parameter of the A/D converter" for the exact values of the microcontroller under consideration.

5.2 Accuracy at Sample Time

As described in **"Principle of Conversion" on Page 13**", a total conversion is divided into two phases:

- Sample phase
- Charge-redistribution phase

The total accuracy of the A/D converter result depends on three elements:

- Specified TUE and the accuracy of the A/D converter itself
- Accuracy of V_{AREF} and V_{AGND} at the charge-redistribution phase
- Voltage level difference between analog source V_0 and V_{AINSW} ($Error_{ANx}$) at the end of the sample phase

A detailed consideration of the voltage level at C_{AINSW} (or at ANx, respectively) is the condition necessary to determine the correct values for R_{ASRC}, C_{EXT}, sample time, and cycle time of a system.

The worst case voltage deviation (V_0 - V_{AINSW}) for the analog input signal is the maximum voltage difference between the pre-charge voltage of C_{AINSW} (approximately V_{AREF} / 2) and V_0 at the beginning of the sample phase. This case is given for $V_0 = V_{AREF}$ or $V_0 = V_{AGND}$.

The following figure shows the absolute voltage difference between V_0 and C_{AINSW} ($|V_0 - V_{AREF} / 2|$) at the beginning of the sample phase.

The formulas in this document are all related to the absolute maximum possible $V_0 = V_{AREF}$. The result can also be transformed to $V_0 = V_{AGND}$.

Voltages used in the calculations are all referred to V_{AGND}.

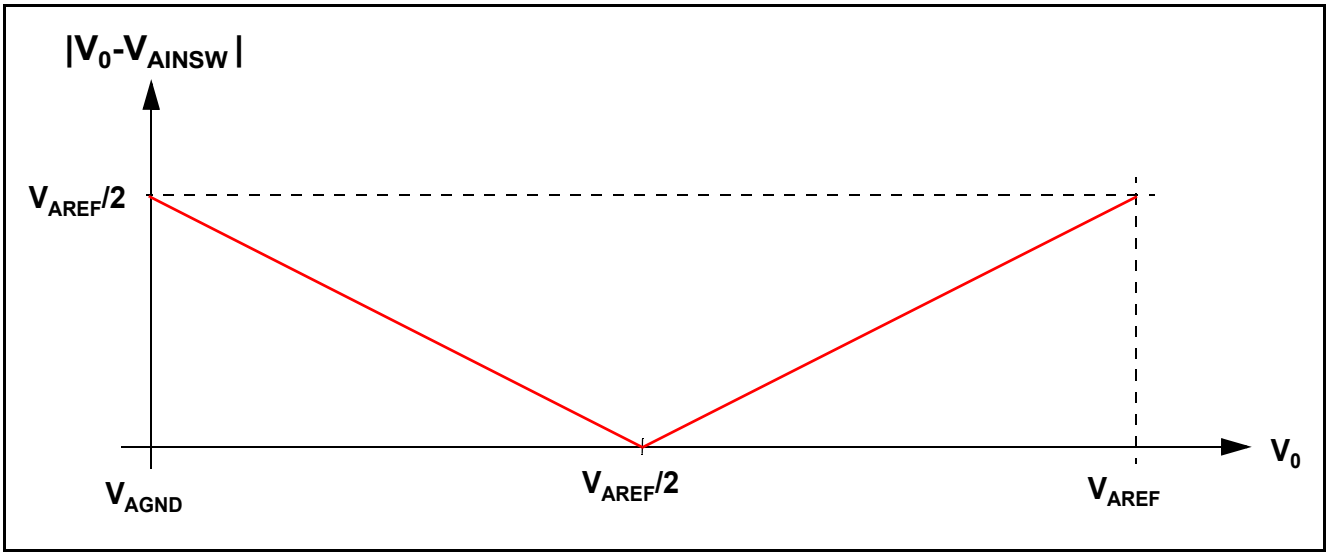

Figure 10 Voltage Difference between V_0 and V_{AINSW} at the start of the Sample Time

*Note: The assumed error ($Error_{ANx}$) used in this chapter (**Analog Input Circuitry Calculation (AN0 ... ANy)**) for the calculation examples references the allowed maximum input voltage at ANx ($V_{AINSWx} = V_{AREF}$). For input voltages at ANx smaller than V_{AREF} the additional inaccuracy at V_{AINx} is proportionally less than the value of $Error_{ANx}$ used in the example calculations.*

The real additional inaccuracy at V_{AINx} is:

$$Error_{ANx\_real} = (V_{AINx} / V_{AREF}) * Error_{ANx}$$

with the condition:

$$V_{AGND} \leq V_{AINx} \leq V_{AREF}$$

5.3 Charge Flow during Sample Time

The input impedance of the A/D converter is mainly capacitive (C_{AINSW}) with a resistive part R_{AIN}.

However this capacitance applies only to the selected analog input pin ANx during the sample time. For the remaining time the inputs are extremely high impedance (typical leakage currents are in the range of some 10 nA for example).

Note: Please refer to 'Input leakage current of the ADC' in the appropriate data sheet for the microcontroller under consideration for more detailed information.

Using a simplified model, two different sequential processes are running during the sample phase.

- C_{AINSW} is charged from C_{EXT} and the voltages at C_{AINSW} and C_{EXT} are assigned the same value
- The common voltage at C_{AINSW} and C_{EXT} is adjusted to V_0 via the resistance of the analog source R_{ASRC}

Depending on the phases of the A/D converter, different time constants ('t') have to be considered:

- t_1 : Time constant at the beginning of the sample time
  - Contains C_{AINSW}, C_{EXT} and R_{AIN}
- t_2 : Time constant during sample time
  - Contains C_{AINSW}, C_{EXT} and R_{ASRC}
- t_3 : Time constant during and after the charge-redistribution phase
  - Contains C_{EXT} and R_{ASRC}

5.3.1 Charge Balance between C_{AINSW} and C_{EXT}

The electrical model for t_1 is shown in **Figure 11**.

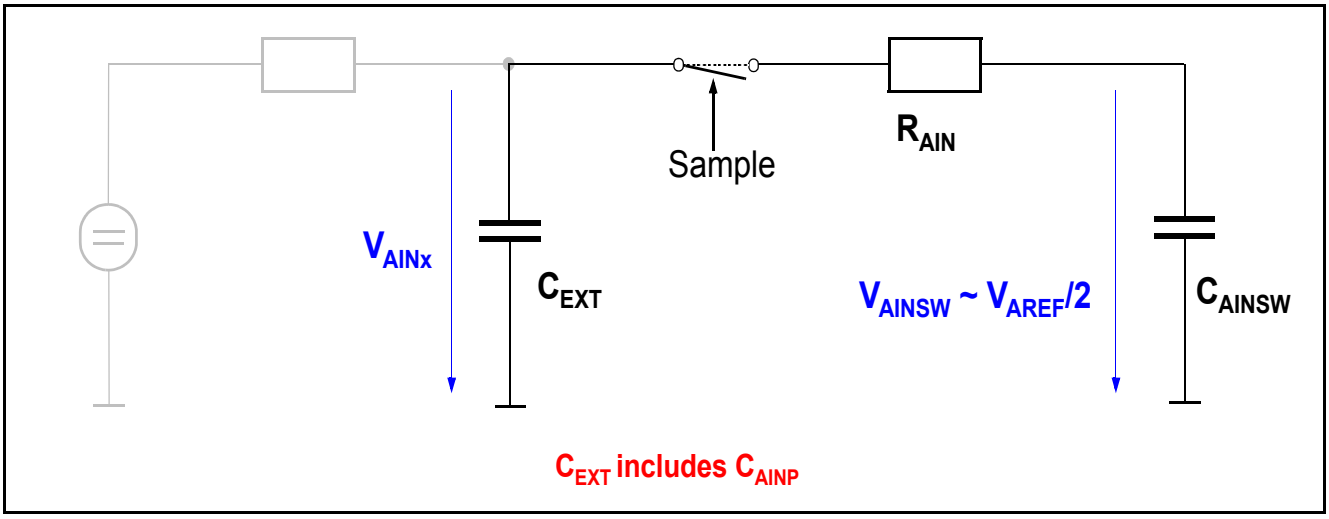

Figure 11 Electrical Model of the A/D Converter during t_1

The voltage at C_{AINSW} before the 'Sample' switch is closed, is approximately $V_{AREF}/2$ because of pre-charging C_{AINSW} at the end of the conversion.

The voltage V_{AINx} at C_{EXT} is nearly V_0 depending on the cycle time of the conversion.

When the 'Sample' switch is closed, then a charge balance is made between C_{AINSW} and C_{EXT}, with the time constant t_1 (See **Figure 11**).

*Note: **Figure 13** shows the corresponding waveform at ANx.*

(1)

$$t_1 = R_{AIN} \cdot \frac{C_{AINSW} \cdot C_{EXT}}{C_{AINSW} + C_{EXT}}$$

Depending on the microcontroller, the values for C_{AINSW} are typically in the range of:

- C_{AINSW} : 5 pF up to 20 pF

The values for R_{AIN} are typically in the range of:

- R_{AIN} : 500 Ω up to 2000 Ω

Typical combinations of an A/D converter are:

- C_{AINSW} = 5 pF and R_{AIN} = 2000 Ω
- C_{AINSW} = 20 pF and R_{AIN} = 1500 Ω

These combinations result in maximum values for t_1 of 10 ns and 30 ns, because R_{AIN} and C_{AINSW} are constant values of the A/D converter.

For the calculation of the sample time, the duration of time constant t_1 is in many cases negligible.

- After 7.6*t the voltage error is less than 0.5 LSB_{10}
- After 9*t the voltage error is less than 0.5 LSB_{12}

The following table gives typical values of 7.6*t_1 and 9*t_1.

Table 1 Typical Values for 7.6*t_1 and 9*t_1

C_{EXT}	1 pF	10 pF	100 pF	1 nF	10 nF	100 nF	1 µF
7.6*t_1 @ (R_{AIN}=2kW, C_{AINSW}= 5 pF)	1.7 ns	6.7 ns	9.5 ns	10 ns	10 ns	10 ns	10ns
9*t_1 @ (R_{AIN}=2kW, C_{AINSW}= 5 pF)	15 ns	60 ns	86ns	90 ns	90 ns	90 ns	90ns
7.6*t_1 @ (R_{AIN}=1.5kW, C_{AINSW}=20 pF)	1.4 ns	10 ns	25ns	29 ns	30 ns	30 ns	30ns
9*t_1 @ (R_{AIN}=1.5kW, C_{AINSW}=20 pF)	13 ns	90 ns	225ns	265 ns	269 ns	270 ns	270ns

The charge balance between C_{AINSW} and C_{EXT} causes a voltage jump V_Δ at the analog input ANx.

Depending on the voltage on ANx when the sample phase starts, the voltage can be increased or decreased.

The example in **Figure 13** uses the worst case $V_0 = V_{AREF}$.

At the end of 7.6*t_1 the voltage at ANx is reduced (or increased) by the value V_Δ with an accuracy of 0.5 LSB_{10} and after 9*t_1 with an accuracy of 0.5 LSB_{12}.

Using this simplified model the charge balance between C_{EXT} and C_{AINSW} results in the formula for V_Δ:

(2)

$$V_\Delta = \frac{C_{AINSW} \cdot (V_0 - V_{CAINSW})}{C_{AINSW} + C_{EXT}}$$

Table 2 Typical Values for the Voltage Jump V_Δ with Pre-charge disregarding R_{ASRC}: V_0 - V_{CAINSW} = 2.5 V and V_0 = V_{AREF}

CEXT	1 pF	10 pF	100 pF	1 nF	10 nF	100 nF	1 µF
V_Δ [1)]	2.4 V	1.7 V	400 mV	50 mV	5 mV	0.5 mV	0.05 mV
V_Δ [2)]	2.1 V	0.8 V	120 mV	12 mV	1.2 mV	0.1 mV	0.01 mV

[1)] Voltage Jump V_Δ@ C_{AINSW} = 20 pF and R_{AIN} = 1500 Ω
[2)] Voltage Jump V_Δ @ C_{AINSW} = 5 pF and R_{AIN} = 2000 Ω

5.3.2 Charge of C_{AINSW} and C_{EXT} via R_{ASRC}

The following figure shows the simplified electrical model during sample time with t_2.

In this model R_{AIN} is neglected because in typical systems R_{ASRC} >> R_{AIN}.

The voltage at C_{AINSW} and C_{EXT} is defined by V_0 and V_Δ at the beginning of the second phase ('start-voltage' = V_0 - V_Δ).

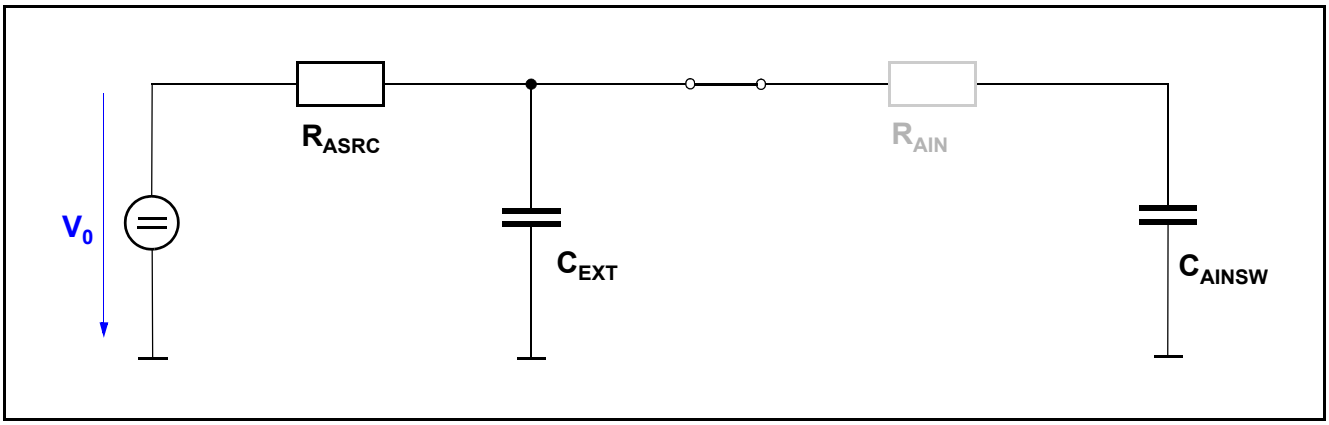

Figure 12 Electrical Model of the A/D Converter during t_2

After V_Δ has reached the absolute maximum value, C_{EXT} and C_{AINSW} are charged via R_{ASRC} from V_0 with the time constant t_2.

(3)

$$t_2 = R_{ASRC} \cdot (C_{AINSW} + C_{EXT})$$

5.4 R_{ASRC} Calculation with (0 pF < C_{EXT} < (2^r - 1) * C_{AINSW})

To ensure reliable results, the input capacitance C_{AINSW} must be completely charged to the desired value during sample time. This is then digitized by the A/D converter.

Under worst-case conditions, the input capacitance must be charged or discharged by half the input voltage when $V_0 = V_{AREF}$ or when $V_0 = V_{AGND}$.

The input capacitance C_{AINSW} of the A/D converter, the external capacitance C_{EXT} and the resistance of the analog source R_{ASRC} together form an RC lowpass filter, which has the charging function $V_S(t)$. In many systems sample time t_S >> t_1, therefore t_1 is neglected in the formula for $V_S(t)$. The waveform is shown in **Figure 13**.

(4)

$$V_s(t) = V_{AREF} - V_\Delta \cdot e^{\frac{-t}{t_2}}$$

The voltage on ANx at the end of the sample time can also be described with the formula $V_S(t_S)$.

The $Error_{ANx}$ describes the maximum deviation allowed between the voltage on ANx and V_0 when the sample time is finished.

An assumed $Error_{ANx}$ of 0.5 LSB is equivalent to the values shown in the following table:

Table 3 Absolute Values of 0.5 LSB for different A/D Converter Resolutions

Resolution	8-bit	10-bit	12-bit
0.5 LSB @ V_{AREF} = 5 V	9.76 mV	2.44 mV	0.61 mV
0.5 LSB @ V_{AREF} = 3.3 V	6.45 mV	1.61 mV	0.40 mV

(5)

$$V_S(t) = V_{AREF} - Error_{ANx}$$

Now it is possible to calculate the maximum value of the analog source resistance R_{ASRC}.

The formula for R_{ASRC} assumes that R_{AIN} = 0 Ω.

(6)

$$R_{ASRC} = \frac{t_S}{(C_{AIN} + C_{EXT}) \cdot \ln \frac{V_\Delta}{Error_{ANx}}}$$

The formula is only valid for: $V_\Delta / Error_{ANx} > 1$

An assumed maximum $Error_{ANx}$ = LSB / 2 leads to $C_{EXT} < (2^r - 1) * C_{AINSW}$

Depending on the A/D converter resolution the relationships between C_{EXT} and C_{AINSW} are:

8-bit resolution: 0 pF < C_{EXT} < 255 * C_{AINSW}
10-bit resolution: 0 pF < C_{EXT} < 1023 * C_{AINSW}
12-bit resolution: 0 pF < C_{EXT} < 4095 * C_{AINSW}

Note: This is only an approximate estimation. The accuracy of the model decreases as the value for C_{EXT} increases, but the model explains the principle behavior of the circuit.

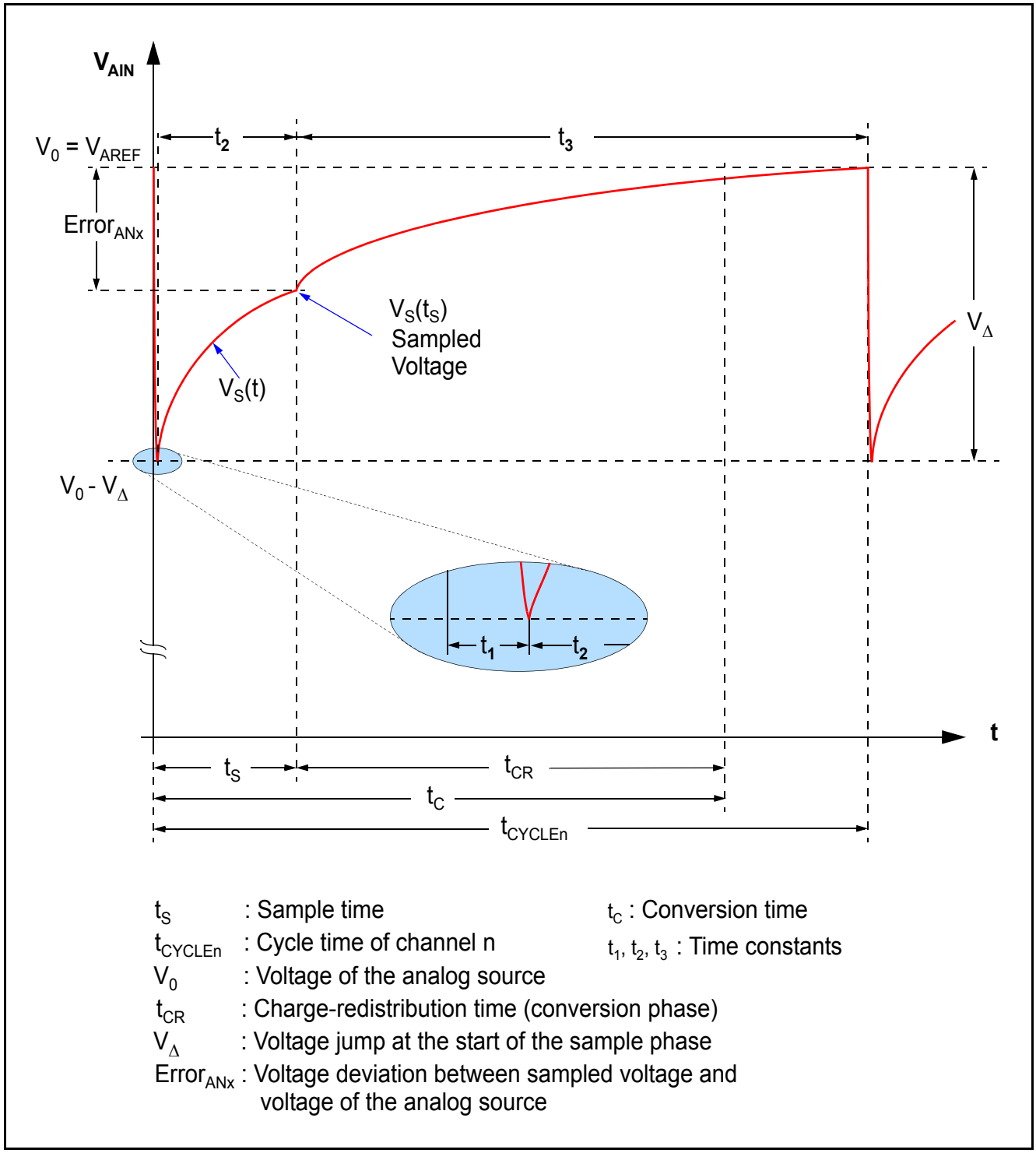

Figure 13 Voltage Waveform at ANx

5.4.1 Charge-Redistribution Time

During the charge-redistribution time, the ‘Sample’ switch is open and the external capacitance C_{EXT} is charged via the resistor of the analog source R_{ASRC}.

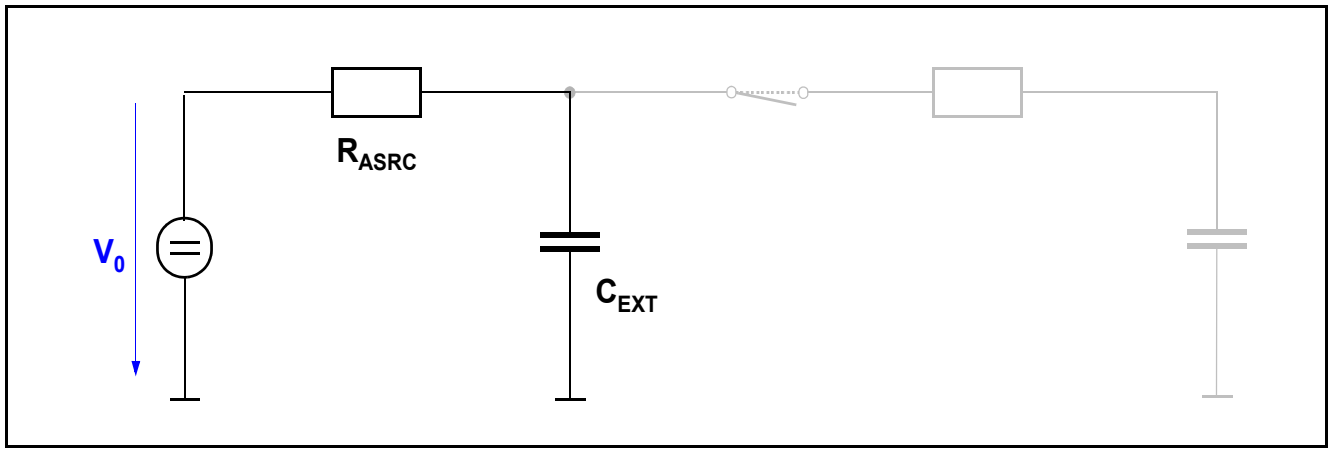

Figure 14 Electrical Model of the A/D Converter during t_3

The time constant during and after charge-redistribution time is t_3.

(7)

$$t_3 = R_{ASRC} \cdot C_{EXT}$$

While the external capacitance C_{EXT} is charged via R_{ASRC}, the A/D converter performs the Successive Approximation (charge-redistribution). This is the transformation of the analog voltage into a digital value. The reference for the transformation is the reference voltage at pin V_{AREF} referred to V_{AGND}. It is very important for an exact conversion result to hold the reference voltage and the reference ground on a constant level during the charge-redistribution. See also **“Reference Voltage Circuitry Calculation (V_{AREF} and V_{AGND})” on Page 39**.

5.4.2 Cycle Time

The cycle time t_{CYCLEn} is the duration from the start of a conversion to the next conversion start of the same analog channel. The following figure shows the relationship between the conversion time of an analog channel and the cycle time.

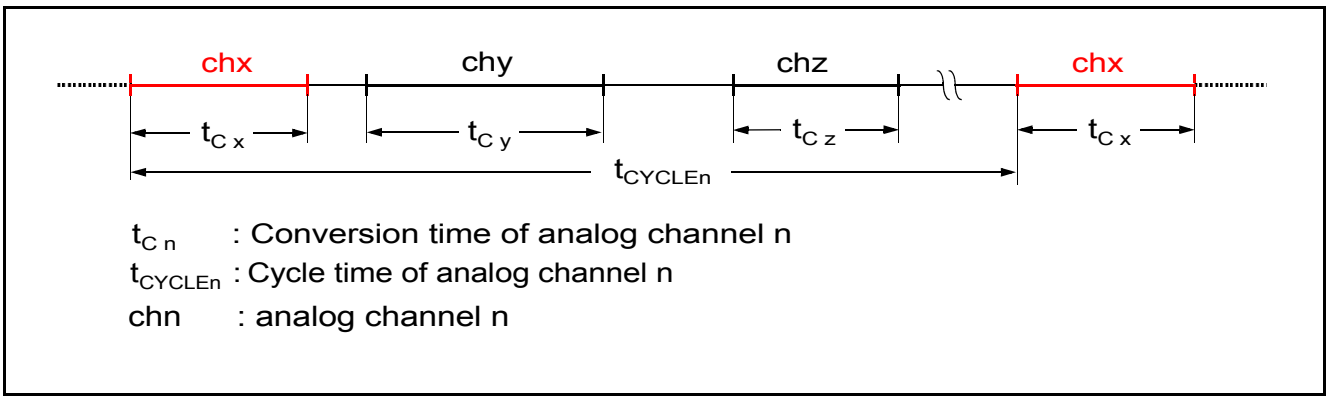

Figure 15 Cycle Time

For continuous conversion mode of a channel, the conversion time t_C can be equal to the cycle time t_{CYCLEn}.

The cycle time of consecutive conversions is important for the calculation of the voltage on C_{EXT} at the start of the next conversion. The voltage difference between the analog source V_0 and the analog input ANx at the start of a conversion should be 0 V or negligible.

The recommendation is:

(8)

$$t_{CYCLE} \geq 9 \cdot t_3 + t_S$$

*Note: After 9 * t_3 the remaining deviation from V_0 is 0.012% (~0.5 LSB_{12}) of the assumed ErrorANx for $V_S(t_S)$. Using 7.6 * t_3 the remaining deviation from V_0 is 0.049% (~0.5 LSB_{10}) of the assumed ErrorANx for $V_S(t_S)$.*

5.4.3 Calculation Example with (0 pF < C_{EXT} < (2^r -1) * C_{AINSW}) and r = 12

The assumed values used in the example are:

C_{AINSW}	= 20 pF	t_S	= 1.5 µs	V_{AREF}	= V_0 = 5 V
R_{AIN}	= 1500 Ω	t_C	= 2.3 µs	r	= 12 (12-bit resolution)
C_{EXT}	= 200 pF				
$Error_{ANx}$	= 0.5 LSB_{12} = V_{AREF} / 4096	$Error_{ANx}$	= 0.61 mV		

The calculation results in the values for R_{ASRC} and t_{CYCLEn}.

5.4.3.1 Resistance of the Analog Source R_{ASRC}

The voltage jump V_Δ during the sample phase is calculated as:

$$V_\Delta = (C_{AINSW} * (V_{AREF} - V_{AREF} / 2)) / (C_{AINSW} + C_{EXT})$$
$$V_\Delta = (20\ pF * (5\ V - 2.5\ V)) / (20\ pF + 200\ pF)$$
$$V_\Delta = 227\ mV$$

The maximum allowed resistance of analog source R_{ASRC} is then calculated:

$$R_{ASRC} = t_S / ((C_{AINSW} + C_{EXT}) * \ln(V_\Delta / Error_{ANx}))$$
$$R_{ASRC} = 1.5\ \mu s / ((20\ pF + 200\ pF) * \ln(227\ mV / 0.61\ mV))$$
$$R_{ASRC} = 1152\ \Omega$$

The table shows the different results of R_{ASRC} with the assumed values used in the example.

Table 4 Maximum Values for R_{ASRC} and different C_{EXT}

C_{EXT}[pF]	1	20	40	60	80	100	150	200	250	500	1000	10000
R_{ASRC} [kW]	8.6	4.9	3.5	2.7	2.2	1.9	1.4	1.2	1.0	0.6	0.35	0.07

*Note: The capacitive load at the analog inputs ANx should be as small as possible because it reduces the allowed resistance of the analog source R_{ASRC} (as shown in **Table 4**). The only exception is the use of a very high value for the external capacitance C_{EXT}, which supplies the A/D converter with the necessary charge during the sample phase.*

5.4.3.2 Cycle Time t_{CYCLEn}

The recommended minimum value of the cycle time is:

$$t_{CYCLEn} = 9 * R_{ASRC} * C_{EXT} + t_S$$
$$t_{CYCLEn} = 9 * 1152\ \Omega * 200\ pF + 1.5\ \mu s$$
$$t_{CYCLEn} = 3.6\mu s$$

The calculated cycle time t_{CYCLEn} is longer than the conversion time t_C and, in that case, continuous conversion of this analog channel is only possible by inserting a waiting period to charge the external capacitance C_{EXT}.

5.5 R_{ASRC} Calculation with ($C_{EXT} > (2^r - 1) * C_{AINSW}$)

This is the typical method of connecting a signal to the analog input. The selected external capacitance has to be high enough that the total charge, which is necessary to load the internal C-net (C_{AINSW}) of the A/D converter, is provided by the external capacitor C_{EXT}.

The considerations outlined in the next subsection (**"External Capacitance C_{EXT}" on Page 28**) use a value for the external capacitance C_{EXT} with respect to the assumed maximum $Error_{ANx}$ caused by discharging C_{EXT} during sample time. The cycle time t_{CYCLEn} has to be long enough to reload the external capacitor C_{EXT} before starting the next sample time.

5.5.1 External Capacitance C_{EXT}

The calculation of the external capacitance C_{EXT} is based on the assumption that $V_{AREF} - V_\Delta$ is the sampled voltage and V_Δ is the maximum allowed $Error_{ANx}$ (See **Figure 16 "Voltage V_{AINx} with CEXT > 2^r * C_{AINSW} and periodical Conversions" on Page 30**). After the charge balance which causes the voltage drop V_Δ, the voltage variation at the capacitors during the sample phase is extremely small. This is because of the time constant t_3 ($t_3 = R_{ASRC} * C_{EXT}$) which is almost in the ms range, and the voltage drop which is in the mV range.

The example to determine the value of the external capacitance C_{EXT} is calculated with the assumption of a maximum allowed error, $Error_{ANx} = LSB_r / 2$.

$$Error = LSB_r / 2$$
$$Error = V_{AREF} / (2^r * 2)$$
$$Error > V_\Delta = (C_{AINSW} * (V_{AREF} - V_{AREF} / 2)) / (C_{AINSW} + C_{EXT})$$

Condition for the external capacitance:

(9)

$$C_{EXT} > (2^r - 1) \cdot C_{AINSW}$$

Depending on the A/D converter resolution the relationship between C_{EXT} and C_{AINSW} is:

8-bit resolution: $C_{EXT} > 255 * C_{AINSW}$
10-bit resolution: $C_{EXT} > 1023 * C_{AINSW}$
12-bit resolution: $C_{EXT} > 4095 * C_{AINSW}$

The condition $C_{EXT} > (2^r - 1) * C_{AINSW}$ allows the choice of a very short sample time t_S because of the small time constant t_1. **Table 1** can be used to help with the appropriate selection of a sample time. Note that the value of R_{ASRC} has a direct influence on the conversion cycle time t_{CYCLEn}.

5.5.2 Cycle Time t_{CYCLEn}

The calculation of the cycle time takes into account that the external capacitor is not totally charged to the voltage of the analog source V_0 (worst cases are $V_0 = V_{AREF}$ or $V_0 = V_{AGND}$), but a small voltage rest V_R is missing (See **Figure 16 "Voltage V_{AINx} with CEXT > 2^r * C_{AINSW} and periodical Conversions" on Page 30**).

With the condition C_{AINSW} << C_{EXT} the formula for V_Δ can be simplified:

$$V_\Delta = (C_{AINSW} * (V_{AREF} - V_{AREF}/2)) / (C_{AINSW} + C_{EXT})$$
$$V_\Delta \sim C_{AINSW} * V_{AREF} / (2 * C_{EXT})$$

The condition $V_\Delta + V_R \le Error_{ANx}$ with $V_R = V_{AREF} - V_C(t_{CYCLEn})$

is based on **Figure 16**.

The charge curve $V_C(t)$ of the capacitor C_{EXT} via the resistance of the analog source R_{ASRC} is:

(10)

$$V_C(t) = V_{AREF} - Error_{ANx} \cdot e^{\frac{-t}{t_3}}$$

With an assumed maximum allowed error of LSB_r / 2 ($Error_{ANx} = (V_{AREF} / 2^r) / 2$) and with $t_3 = R_{ASRC} * C_{EXT}$ the formulas result in the relation:

(11)

$$t_{CYCLE} \ge R_{ASRC} \cdot C_{EXT} \cdot \ln \frac{C_{EXT}}{C_{EXT} - (2^r \cdot C_{AINSW})}$$

This formula is only valid for $C_{EXT} > 2^r * C_{AINSW}$

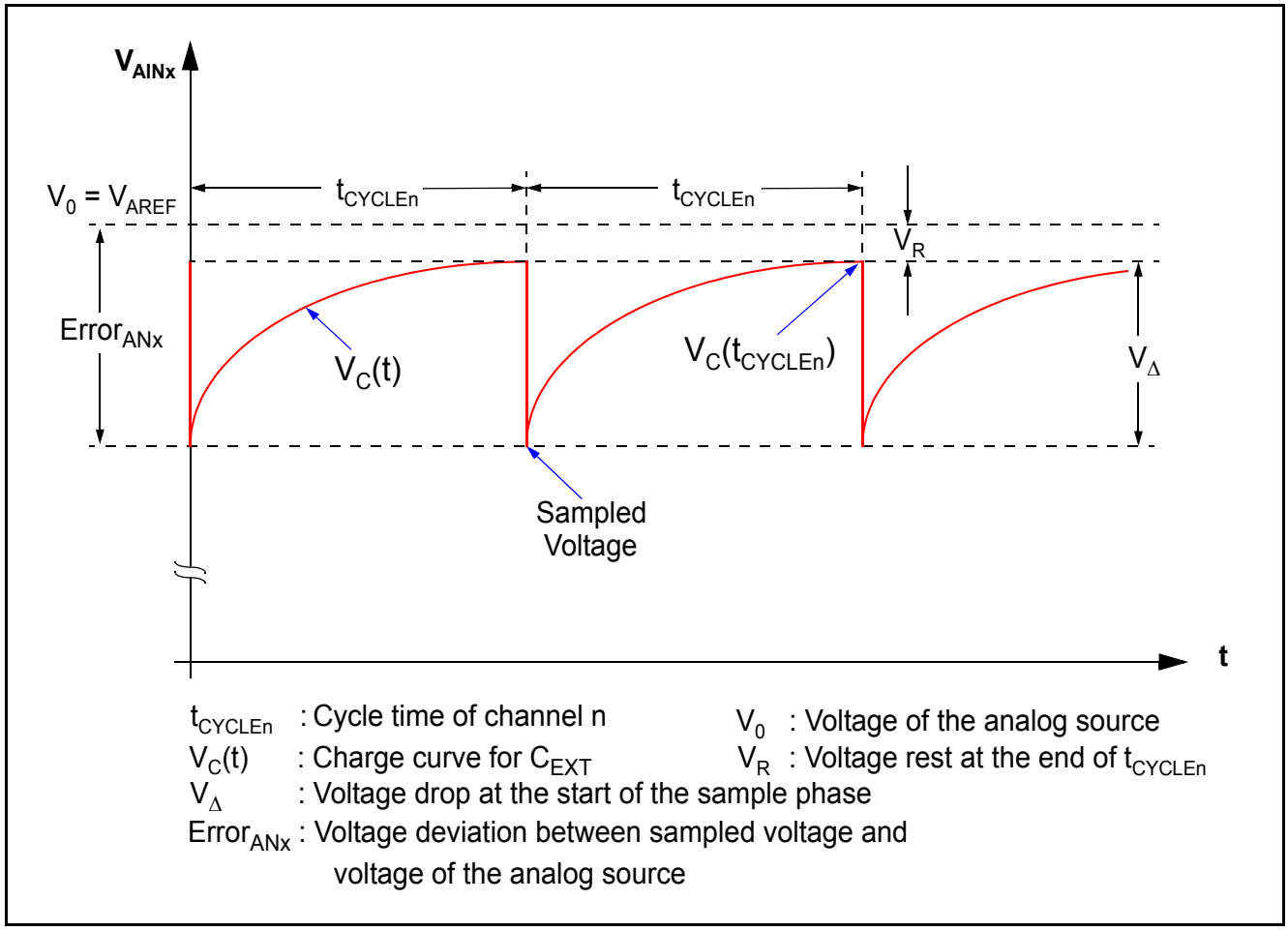

Figure 16 Voltage V_{AINx} with $C_{EXT} > 2^r * C_{AINSW}$ and periodical Conversions

5.5.3 Cutoff Frequency f_C

The resistance of the analog source R_{ASRC} and the external capacitance C_{EXT} act as a low-pass filter with the cutoff frequency f_C. A check is necessary to determine whether the cutoff frequency fits to the frequency of the analog source.

When the relation between the A/D converter cycle frequency ($f_{CYCLE} = 1 / t_{CYCLEn}$) and the cutoff frequency is $f_{CYCLE} / f_C \sim 0.05$, then the analog signal is damped with ~1 $^0/_{oo}$ (~1 LSB_{10}).

(12)

$$f_C = \frac{1}{2 \cdot \pi \cdot R_{ASRC} \cdot C_{EXT}}$$

Note: If the external circuit reaches the cutoff frequency then the voltage of the analog source V_0 is damped with the factor -3 dB ($V_{AIN} \sim 0.7 * V_0$ @ cutoff frequency f_C).

5.5.4 Calculation Example with (C_{EXT} > (2^r - 1) * C_{AINSW})

The assumed values used in the example are:

C_{AINSW}	= 20 pF	t_S	= 0.6 µs	V_{AREF}	= V_0 = 5 V
R_{AIN}	= 1500 Ω	t_C	= 1.4 µs	r	= 12 (12-bit resolution)
R_{ASRC}	= 20 kΩ	C_{EXT}	> 4096 * C_{AINSW} = 82 nF	C_{EXT}	= 100 nF
$Error_{ANx}$	= 0.5 LSB_{12} = V_{AREF} / 4096 / 2	$Error_{ANx}$	= 0.61 mV		

The calculations result in the values of cycle time t_{CYCLEn} and cutoff frequency f_C.

The values of the external capacitance C_{EXT} and resistance of the analog source R_{ASRC} are fixed in relation to the cycle time t_{CYCLEn}:

$$t_{CYCLEn} \geq R_{ASRC} * C_{EXT} * \ln(C_{EXT} / (C_{EXT} - 2^r * C_{AINSW}))$$
$$t_{CYCLEn} \geq 20\ k\Omega * 100\ nF * \ln(100\ nF / (100\ nF - 2^{12} * 20\ pF))$$
$$t_{CYCLEn} \geq 3.4\ ms$$

The cutoff frequency is calculated from:

$$f_C = 1 / (2 * \pi * R_{ASRC} * C_{EXT})$$
$$f_C = 1 / (2 * \pi * 20\ k\Omega * 100\ nF)$$
$$f_C = 80\ Hz$$

Table 5 shows calculation results of the cycle time in [ms] for different values of R_{ASRC} with the assumed values of the example ($Error_{ANx}$ = 0.5 LSB_{12}).

Table 5 Cycle Time t_{CYCLEn} for different Values of R_{ASRC} with C_{EXT} = 100nF

R_{ASRC} [kΩ]	1	5	10	15	20	25	30	40	50	100
t_{CYCLEn} [ms]	0.2	0.9	1.7	2.6	3.4	4.3	5.1	6.8	8.6	17.1

Table 6 shows calculation results of the cutoff frequency in [Hz] for different values of R_{ASRC} with the assumed values of the example ($Error_{ANx}$ = 0.5 LSB_{12}).

Table 6 Cutoff Frequency f_C for different Values of R_{ASRC} with C_{EXT} = 100nF

R_{ASRC} [kΩ]	1	5	10	15	20	25	30	40	50	100
f_C [Hz]	1592	318	159	106	80	64	53	40	32	16

5.6 R_{ASRC} Calculation with (C_{EXT} = 0pF)

In this example, which in real systems is hard to realize and which is very sensitive to noise, the external capacitance is neglected. The electrical model is shown in **Figure 17**. It can be used for an approximate estimation of the external components if the value of C_{EXT} is nearly zero pF. The internal C-net capacitance of the A/D converter is directly charged via R_{ASRC} and R_{AIN}.

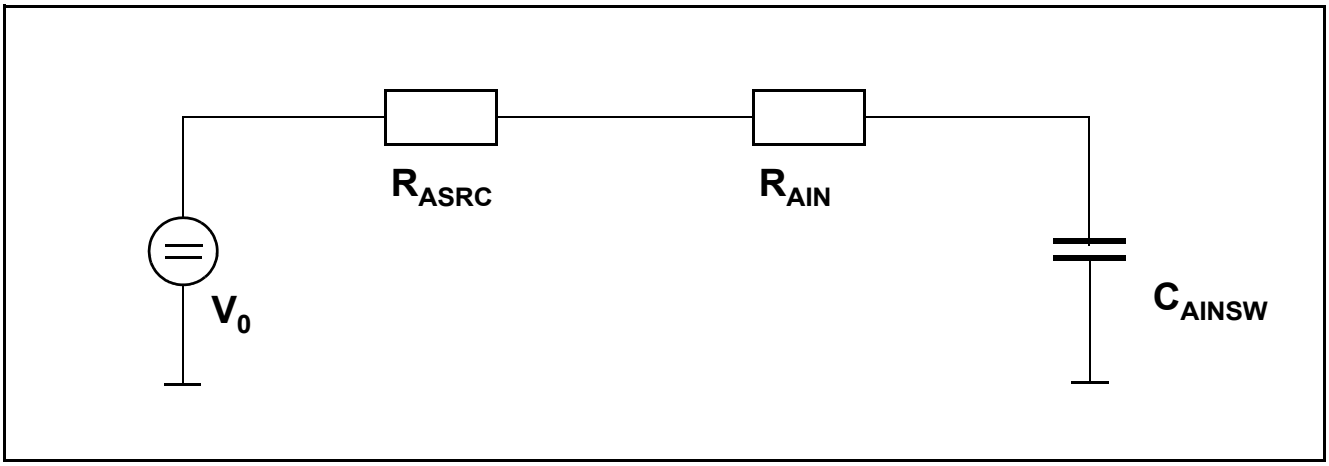

Figure 17 Electrical Model of the A/D Converter during t_2 with C_{EXT} = 0 pF

5.6.1 Resistance of the Analog Source R_{ASRC}

When the external capacitance is C_{EXT} = 0 pF then the time constant t_1 = 0 s and the maximum voltage drop V_Δ at the beginning of the sample time is approximately V_{AREF} / 2, equal to the precharge value of the internal C-net.

$$V_\Delta = (C_{AINSW} * (V_{AREF} - V_{AREF} / 2)) / C_{AINSW}$$
$$V_\Delta = V_{AREF} / 2$$

The resistance of the analog source R_{ASRC}, is calculated with the formula for systems with a small external capacitance but without C_{EXT} and with R_{AIN}.

(13)

$$R_{ASRC} = \frac{t_S}{C_{AINSW} \cdot \ln \frac{V_\Delta}{Error_{ANx}}} - R_{AIN}$$

The calculation of the cycle time is not necessary because during sample time the internal C-net is connected to the analog source. In the other phases of the cycle time the internal C-net is disconnected from the analog source. Therefore no external capacitance has to be charged via R_{ASRC} until the start of the next sample time.

5.6.2 Calculation Example with (C_{EXT} = 0pF)

This example gives an approximate estimation for the allowed maximum of R_{ASRC} if C_{EXT} is nearly zero pF.

The assumed values in the example are:

C_{AINSW}	= 20 pF	t_S	= 1.5 µs	V_{AREF}	= V_0 = 5 V
R_{AIN}	= 1500 Ω	t_C	= 2.3 µs	r	= 12 (12-bit resolution)
C_{EXT}	= 0 pF		precharge voltage:	V_Δ	= V_{AREF} / 2
$Error_{ANx}$	= 0.5 LSB_{12} = V_{AREF} / 4096	$Error_{ANx}$	= 0.61 mV		

The calculation results in the value for R_{ASRC} with $V_\Delta = V_{AREF} / 2$.

$$R_{ASRC} = t_S / (C_{AINSW} * \ln(V_\Delta / Error_{ANx})) - R_{AIN}$$
$$R_{ASRC} = 1.5\ \mu s / (20\ pF * \ln(2.5\ V / 0.61\ mV)) - 1500\ \Omega$$
$$R_{ASRC} = 7516\ \Omega$$

The table shows the maximum values for R_{ASRC} and different sample times with the assumed values of the example:

Table 7 Maximum Values for R_{ASRC} and sample Times t_S @ C_{EXT} = 0 pF

t_S [µs]	0.5	1	1.5	2	3	4	5	6	7	8	9	10
R_{ASRC} [kΩ]	1.5	4.5	7.5	10.5	16.5	22.5	28.6	34.6	40.6	46.6	52.6	58.6

*Note: The leakage current specified in the Data Sheet for the given microcontroller can influence the accuracy of the analog input voltage, when the value of R_{ASRC} exceeds a certain limit. This limit depends on the allowed inaccuracy (V_{AINx}), which is determined by the demands of the system. See also "**"Overload and Leakage Current" on Page 46**".*

6 Analog Input Circuitry Simulation (AN0 ... ANy)

The simplified electrical model used for the calculation of the analog input circuitry described in this document, does contain some inaccuracies, but it can still be used for the start values of an A/D converter circuitry simulation.

A simulation based on the A/D converter block diagram using the specified values from the Data Sheet of the given microcontroller, combined with the external circuitry used, shows the realistic dynamic behavior of the different components.

The simulation examples given here are created with ngspice. Ngspice is an open source SPICE simulator which can be used as a local install or online.

An assessment of the A/D converter input circuitry and software settings (sample and conversion time) can be made by analyzing the voltage difference between the analog source voltage V_0 and the internal C-net voltage V_{AINSW} of the A/D converter. The lower this difference at the end of the sample time t_S, the better the A/D converter input circuitry selection and software settings. This is because at the end of the sample time the voltage at C_{AINSW} is the voltage which is converted to the digital output via Successive Approximation (charge-redistribution phase).

6.1 Analog Input Circuitry Simulation Model

The simulation model given here consists of a typical external circuit with voltage source V_0 and the low pass filter R_{ASRC} and C_{EXT}.

The external capacitance is selected with $C_{EXT} > (2^r-1) * C_{AINSW}$.

Sample time behavior is realized with a sample switch.

The pre-charge voltage behavior is realized with a pre-charge voltage and a pre-charge switch.

The influence of the leakage current can be verified by adapting I_{OZ} to the Data Sheet values of the appropriate microcontroller.

The model circuitry is shown in **Figure 18 “Simplified Model of the A/D converter Input Circuitry” on Page 35**.

The assumed values for the example are:

C_{AINSW_MAX}	= 20 pF	maximum switched capacitance
R_{AIN_MAX}	= 1500 Ω	distributed to R_{in} = 500 Ω and R_{on} = 1000 Ω (sample switch)
R_{ON}	= 1000 Ω	sample switch on resistance
t_S	= 600 ns	sample time
t_C	= 1.4µs	conversion time
t_{CYCLEn}	= 3400 µs	cycle time, time until start of the next conversion of the same channel
$V_{PRECHARGE}$	= 2.5 V	precharge voltage at the end of the conversion time
C_{EXT}	= 100 nF	external analog input capacitance
R_{ASRC}	= 20000 Ω	resistance of the analog source
V_0	= 5 V	is one worst case (or V_0 = 0V) for recharging C_{AINSW} after pre-charging
I_{OZ}	= +/-30 nA	typical leakage source at room temperature
V_LSB10	= 4.995 V	limit voltage V_0 - $1LSB_{10}$ for plot
V_LSB12	= 4.9988 V	limit voltage V_0 - $1LSB_{12}$ for plot

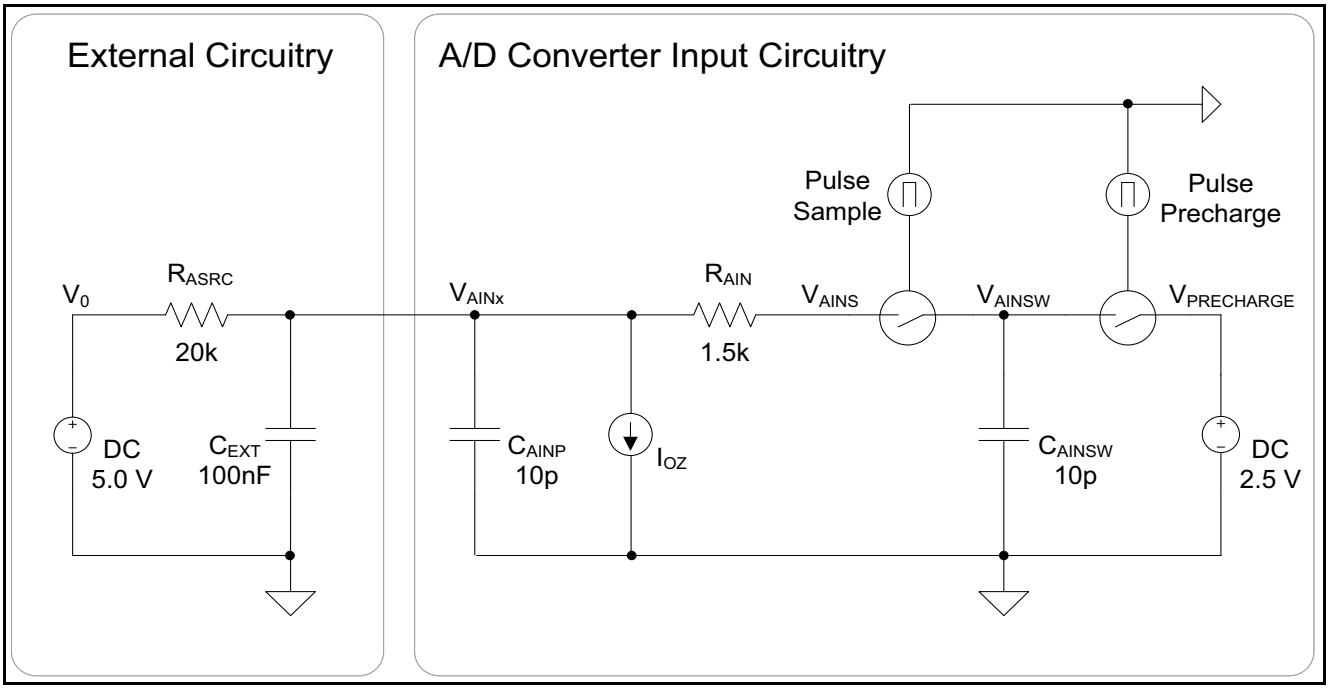

Figure 18 Simplified Model of the A/D converter Input Circuitry

Analog Input Circuitry Simulation Netlist for ngspice

```
* ngspice file: ADC_model.asc
* ADC Input Circuitry
Rasrc  V0     Vainx 20k
Rin    Vainx  Vains 500
Cext   Vainx  0     100n
Cainp  Vainx  0     10p
Cainsw Vainsw 0     20p

*----- sample and precharge control
S1 Vainsw     Vains  sample_on/off    0 ISWITCH
S2 Vprecharge Vainsw precharge_on/off 0 ISWITCH

V_sample_control    sample_on/off    0 PULSE(0 1  10n 5n 5n 600n 3400u)
V_precharge_control precharge_on/off 0 PULSE(0 1 1.2u 5n 5n 190n 3400u)
.model ISWITCH      SW(Ron=1k Roff=10G Vt=0.5)

*----- leakage current
B_leak Vainx 0 I=12n*V(Vainx)-30n

*----- voltages
Vanalog_source V0         0 5.0
V_precharge    Vprecharge 0 2.5
V_LSB12        LSB_12     0 4.9988
V_LSB10        LSB_10     0 4.995

.tran 10u 50m
.end
```

6.2 Simulation Results

Figure 19 and **Figure 20 “Simulation Result with Leakage Current (V_{AINx}, V_0 and V_{LSB_12})” on Page 37** show the simulation results of voltage V_{AINx}, which can be measured at the analog input pin ANx to V_{AGND}. After a certain ‘settling’ time, there is a constant peak to peak amplitude of discharging C_{EXT} during sample time and charging C_{EXT} via R_{ASRC} until the start of the next sample event.

After pre-charging C_{AINSW} to $V_{AREF}/2$ at the end of the conversion, C_{AINSW} has to be charged to V_0 during the sample time via the charge stored in C_{EXT}.

The constant voltage V_{LSB12} shows a limit of V_0 - $1LSB_{12}$ (4.998V).

After the circuitry settling period, the charge for loading C_{AINSW} and the charge for loading C_{EXT} are in balance.

Note that the simulation result in **Figure 19** does not consider the influence of the leakage current. In **Figure 20** a typical leakage current at room temperature is included in the simulation. In this example the maximum additional error contributed by the leakage current is about 0.5 LSB_{12}.

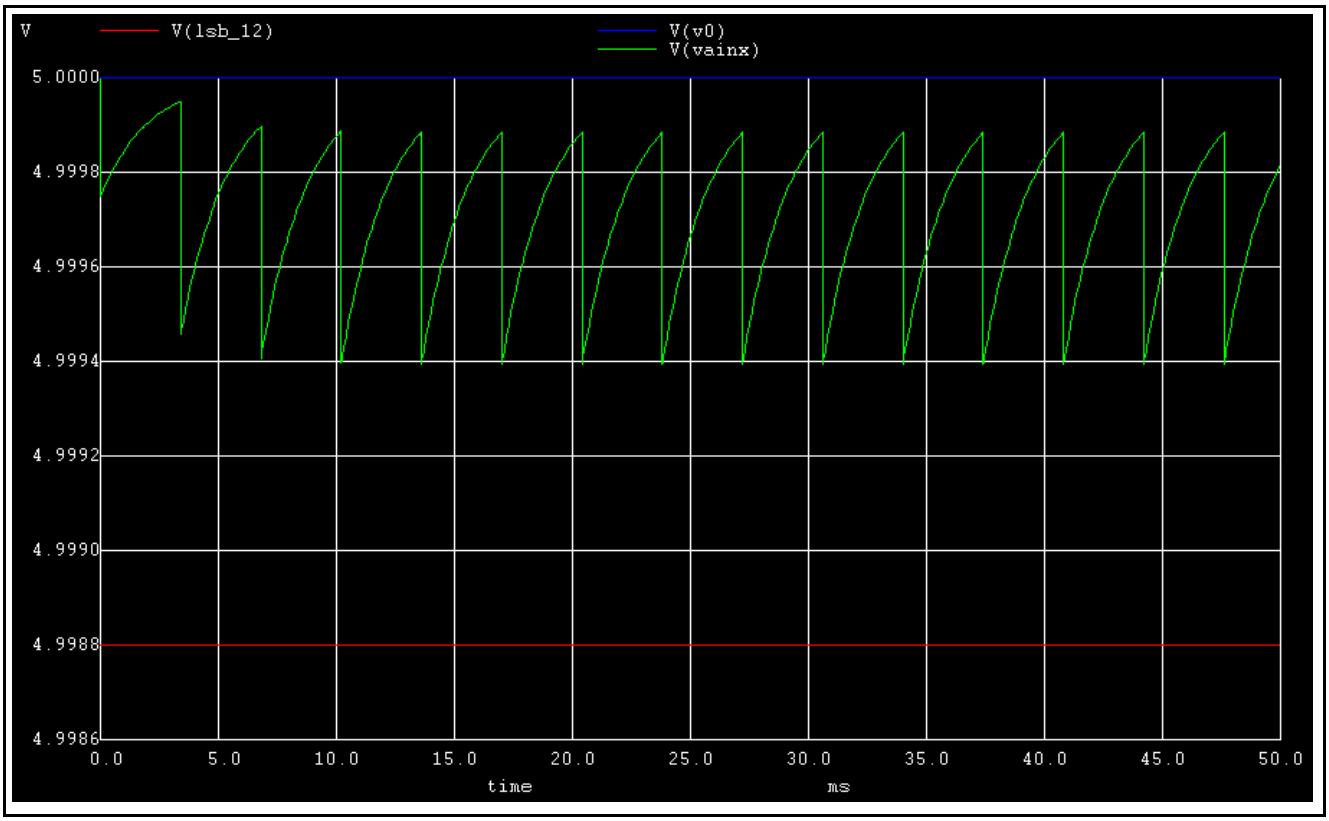

Figure 19 Simulation Result without Leakage Current (V_{AINx}, V_0 and V_{LSB_12})

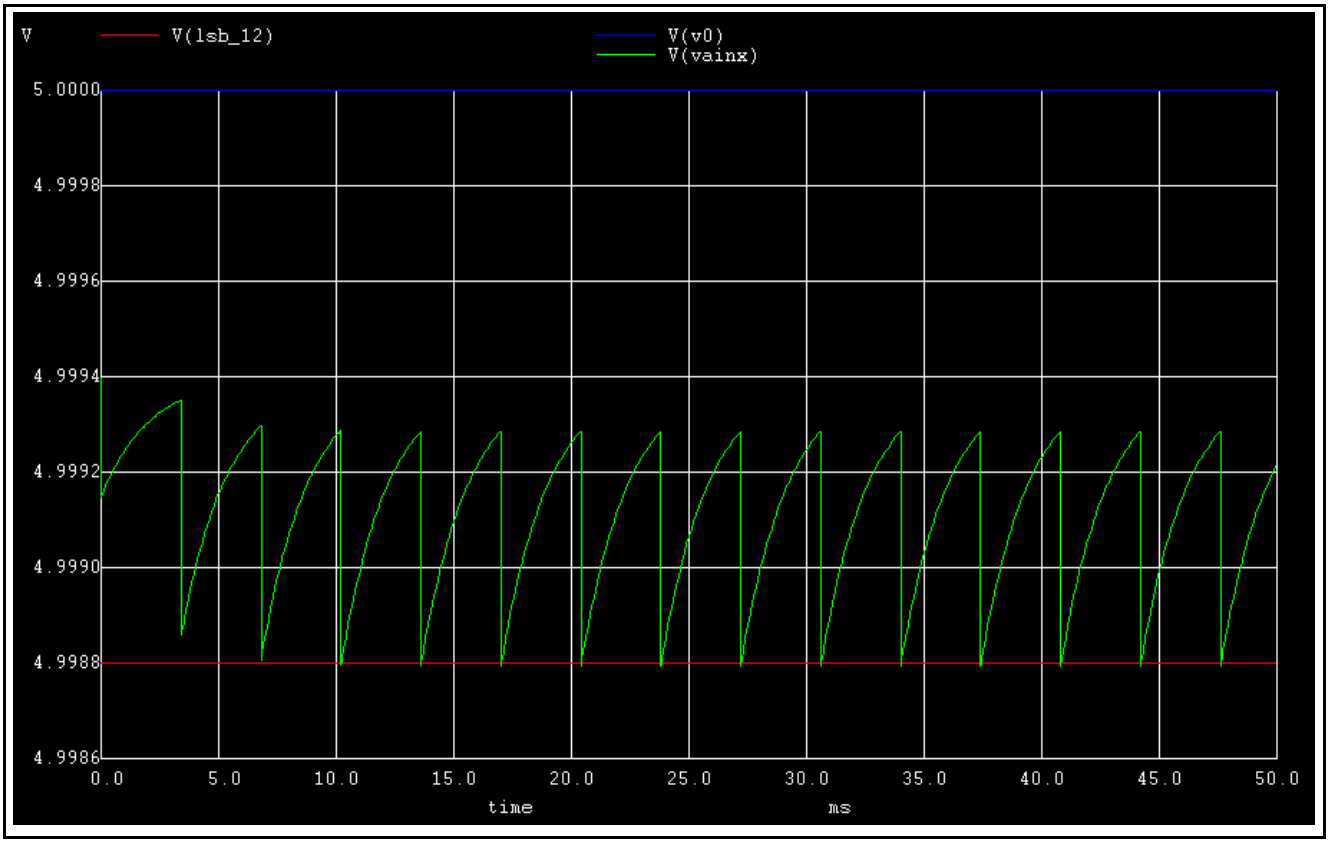

Figure 20 Simulation Result with Leakage Current (V_{AINx}, V_0 and V_{LSB_12})

The simulation results in **Figure 21 "V_{AINSW} without Leakage Current" on Page 38** and **Figure 22 "V_{AINSW} with Leakage Current" on Page 38** show the voltage V_{AINSW} at C_{AINSW} during sample time. This is the voltage which is converted to a digital value while Successive Approximation is running. This value is then transferred to the A/D converter result register.

The constant voltage V_{LSB12} shows the limit of V_0 - $1LSB_{12}$ (4.998V).

The error of the sampled voltage without considering the leakage current is about 0.5 LSB_{12}. With the leakage current considered, it is approximately 1 LSB_{12}. Therefore the analog voltage for conversion at C_{AINSW} is about 1.2mV below the voltage of the analog source V_0.

When V_0 is less than V_{AREF} (V_{AREF} / 2 < V_0 < V_{AREF}) then this "input circuit error" is proportionally less than the 1.2mV shown.

The following analog input circuit parameter changes increase the "input circuit error":

- Increasing R_{ASRC}
- Decreasing sample time
- Decreasing cycle time

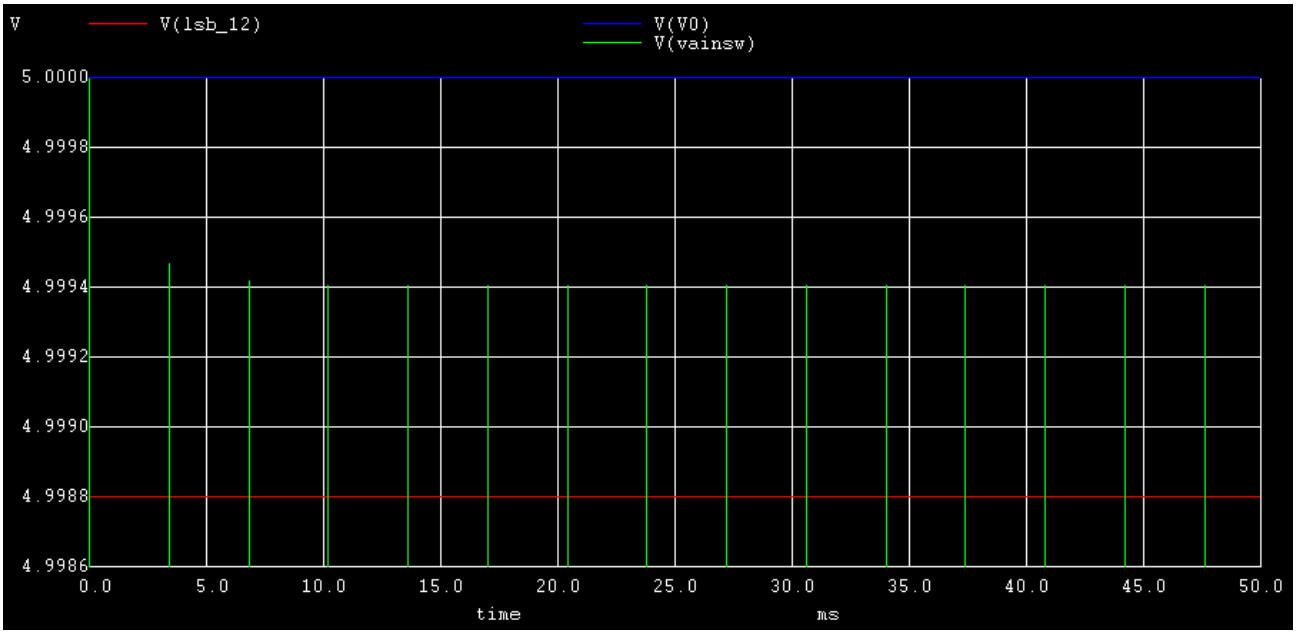

Figure 21 V_{AINSW} without Leakage Current

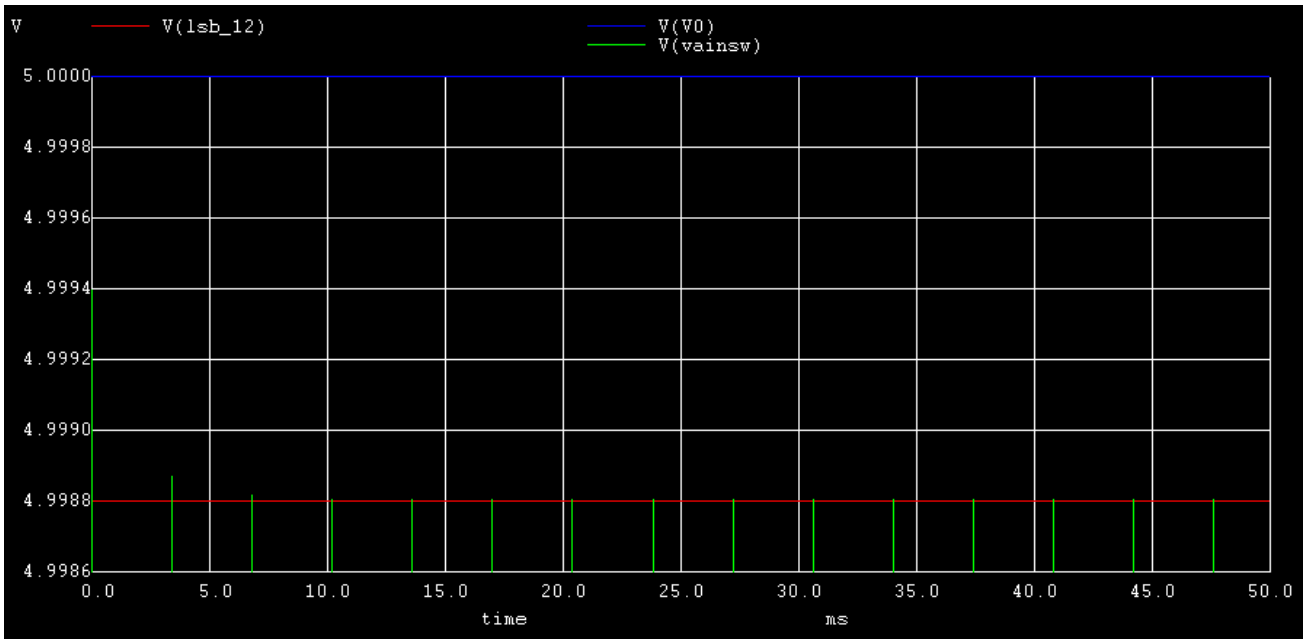

Figure 22 V_{AINSW} with Leakage Current

7 Reference Voltage Circuitry Calculation (V_{AREF} and V_{AGND})

During the charge-redistribution and calibration phases, each group of capacitors from the C-net is individually switched to either V_{AREF} or V_{AGND}. Because of this switching and the resulting charge transfers in the C-net, the A/D converter requires a dynamic current at pin V_{AREF}. As a result, the resistance of the voltage reference source must be low enough to supply the current for the charge-redistribution and calibration phase.

The external circuit at V_{AREF} has a direct influence on the required resistance of the voltage reference. If an external capacitance C_{AREF}, between V_{AREF} and V_{AGND} is used, then the voltage reference only has to supply a small continuous current to charge the external capacitor. The necessary peak current during the charge-redistribution phase is supplied by the external capacitance C_{AREF}. The continuous current and the charge duration (t_{CYCLE}) must be high enough to fill the external capacitance C_{AREF} to a sufficient voltage level before the next charge-redistribution phase starts.

7.1 Electrical Model of the A/D Converter Reference Voltage Input

Figure 23 is a simplified block diagram of the A/D converter reference voltage input. The block diagram includes only the elements necessary for a calculation of the external circuits.

The reference voltage input capacitance C_{REFSW} contains the capacitors of the conversion C-net and all parasitic capacitors which are also switched during the successive approximation phase.

R_{AREF} is the internal series resistance of the A/D converter reference input.

The bit conversion switch represents an analog switch that is periodically closed during successive approximation.

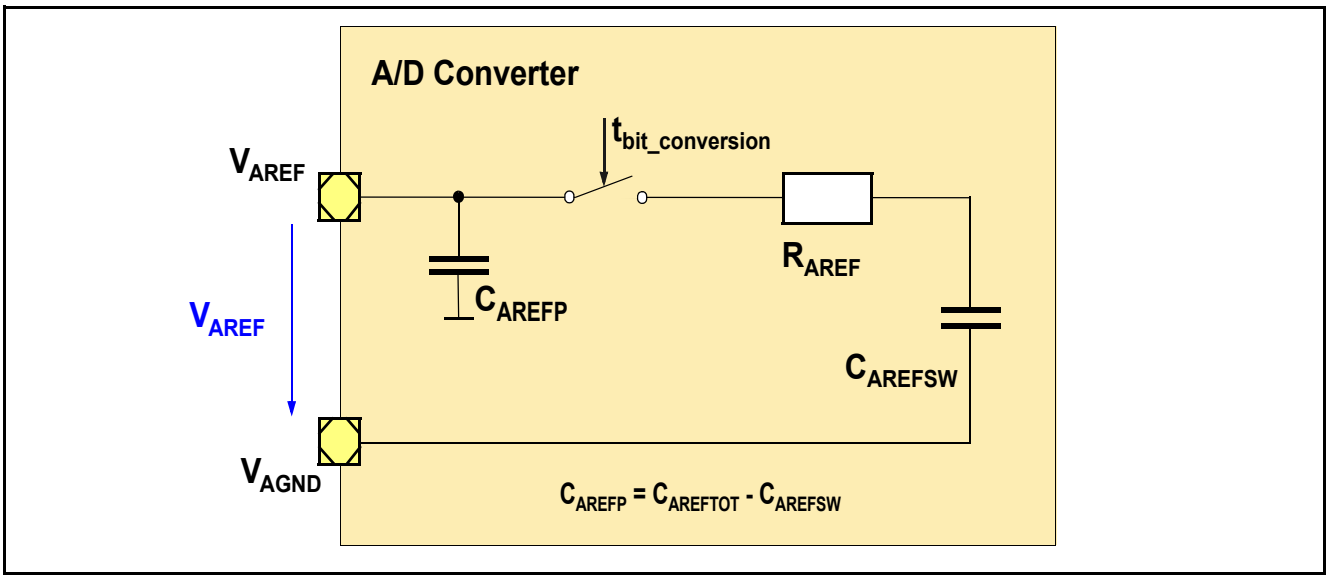

Figure 23 Block Diagram: A/D Converter Reference Voltage Input

The specified values of R_{AREF}, C_{AREFSW} and $C_{AREFTOT}$ are dependent on technology and the type of A/D converter implementation. The order of magnitude for the values is:

C_{AREFSW}	~ 20 pF
$C_{AREFTOT}$	~ 30 pF
R_{AREF}	~ 1000 Ω

Note: Please refer to the relevant microcontroller Data Sheet chapter "Electrical Parameter of the A/D converter" for the exact values.

7.2 Sources for the Voltage Reference

Depending on the requirements, several different kinds of voltage reference can be used in a system. The supply voltage of the microcontroller can be selected for the reference voltage for example, but the accuracy is in the percentage range. The accuracy of an external high precision voltage reference is in the per mille range.

7.2.1 Supply Voltage of the Microcontroller

In most systems, the voltage reference used for the A/D converter is the microcontroller supply voltage V_{DD}. The typical accuracy of a voltage regulator is 2% (please refer to the relevant power semiconductor Data Sheets from Infineon for specific details).

When the digital supply voltage of the microcontroller is used as a voltage reference, the recommendation is to insert a low pass filter between V_{DD} and V_{AREF} (See the figure that follows). The low pass filter has to suppress the supply ripple on V_{DD} to get a noise free reference voltage V_{AREF}. This is necessary because noise on the reference voltage has a direct influence to the accuracy of the A/D converter results.

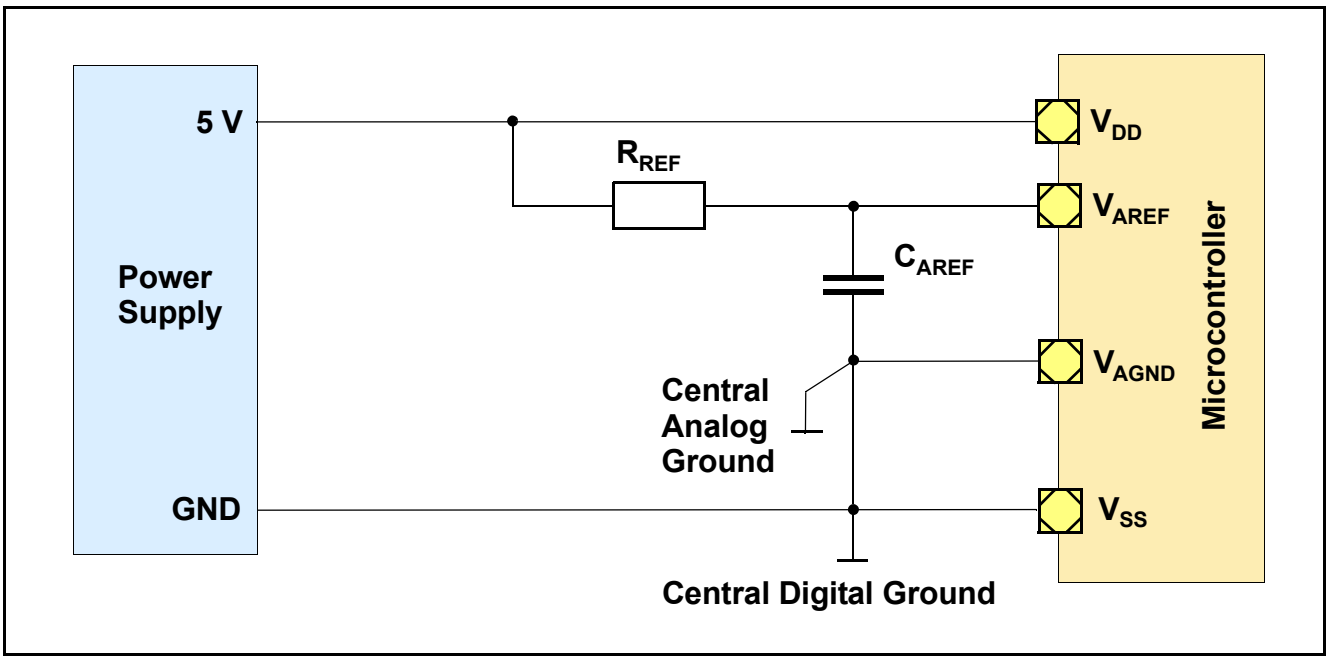

Figure 24 Supply Voltage used for Voltage Reference

The values of the capacitance C_{AREF} and the resistor R_{REF} depend on the characteristics of the system and have a direct influence on overall accuracy.

C_{AREF} provides the necessary charge for loading the MSB of the internal C-net at the start of the charge redistribution phase, and R_{REF} charges C_{AREF} to a sufficient accuracy.

If there is noise on the system supply voltage with a low frequency, then the low pass cut-off frequency can be reduced via an appropriate capacitance added in parallel to C_{AREF}, which stabilizes the voltage reference.

Note: The impedance and the noise caused by the connection between Central Analog Ground and Central Digital Ground should be as low as possible.

7.2.2 External Voltage Reference

The source for an external voltage reference can be a standard supply voltage with increased accuracy. For systems where a high accuracy is required, a high precision voltage reference can be used with a typical accuracy in the range of 2.5 mV ... 20 mV.

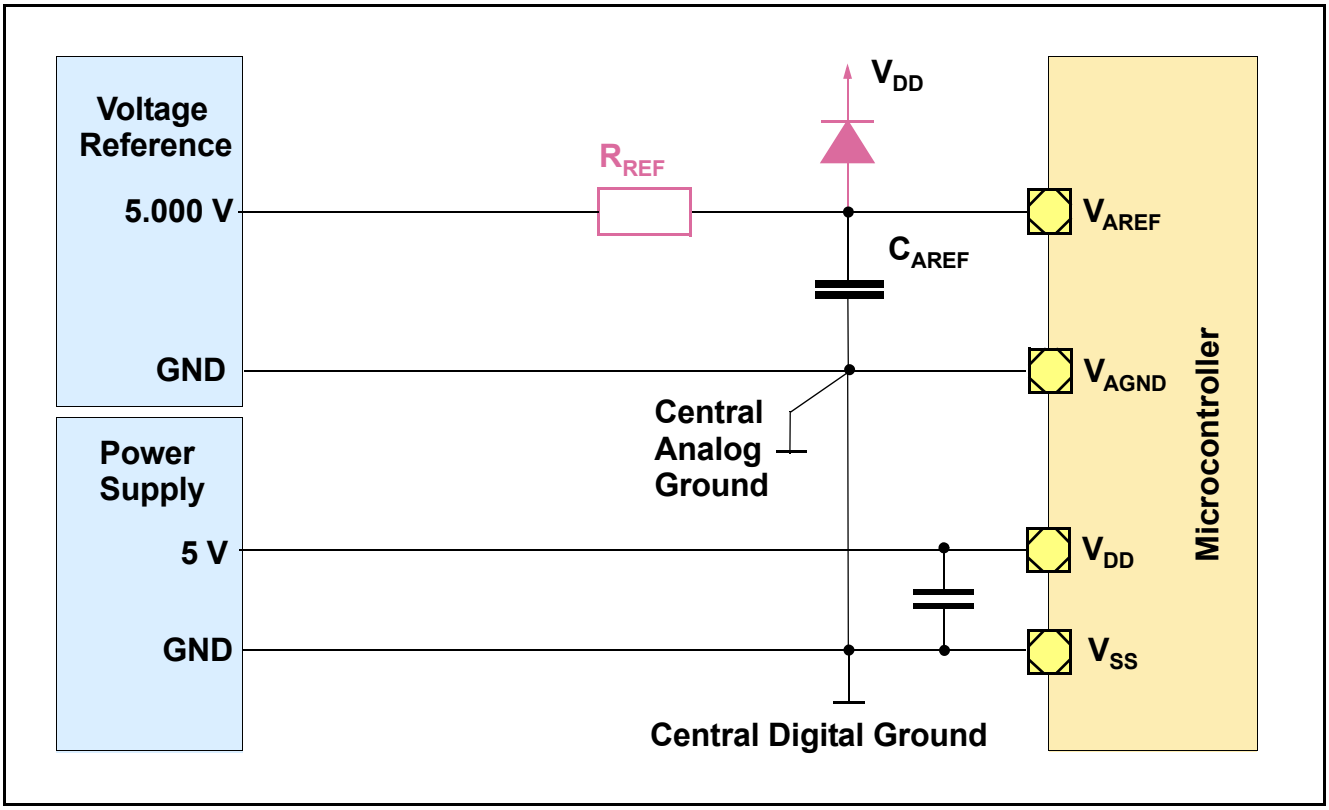

Figure 25 External Voltage Reference

*Note: If the supply voltage of the microcontroller and the voltage reference of the A/D converter are switched on and off at different times, then it is very important that the voltage reference is switched on or off only when the supply voltage of the microcontroller is 'on', otherwise the voltage reference supplies the system with current via the ESD clamp diode. In that case it is necessary to reduce the overload current to the specified absolute maximum ratings (See **"Overload and Leakage Current" on Page 46**). The overload current can be reduced via a resistor or a diode. If the additional external clamp resistor causes an unacceptable additional error at V_{AREF} then an external clamp diode should be used.*

7.3 I_{AREF} Calculation without an External Capacitance C_{AREF}

If there is no external capacitance between V_{AREF} and V_{AGND} then the voltage reference has to directly supply the peak current at the charge redistribution phase. This peak current flows only at the beginning of the MSB conversion and becomes smaller with each converted bit down to the LSB. The minimum current to be supplied by the voltage reference is:

(14)

$$I_{AREF} \geq \frac{V_{RF}}{R_{AREF}}$$

Note: It is not recommended to use a V_{AREF} circuit without an external capacitance C_{AREF} because of the high peak current in the charge redistribution phase.

7.4 R_{REF} Calculation with an External Capacitance C_{AREF}

This calculation is based on the assumption that there is an external capacitance C_{AREF} between V_{AREF} and V_{AGND}. The selected external capacitance has to be high enough such that the total charge, which is necessary to load the internal C-net (C_{AREFSW}) for a total conversion phase, is provided by the external capacitor C_{AREF}.

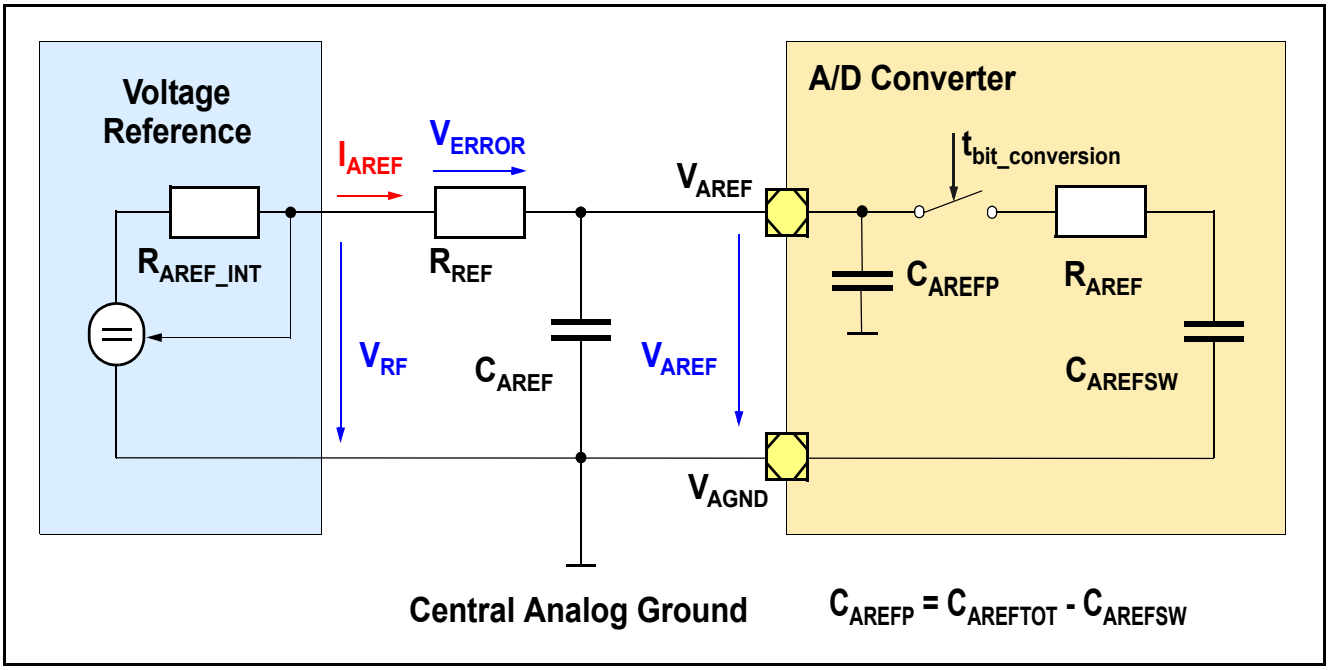

Figure 26 A/D Converter during Conversion Phase with C_{AREF}

The following considerations include the value of the external capacitance C_{AREF} with respect to the assumed maximum voltage error at V_{AREF} ($Error_{AREF}$) caused by C_{AREF}, and the necessary time t_{CYCLE} to reload the external capacitor.

The relationship between the external capacitance C_{AREF}, the internal C-net C_{REFSW} and the assumed maximum error caused by C_{AREF} is:

(15)

$$C_{AREF} \geq 2^{r+E} \cdot \frac{C_{AREFSW}}{2}$$

with:

r = 8 : 8-bit resolution	E = 0 : $Error_{AREF}$ = LSB_r	$Error_{AREF}$ = $LSB_r / 2^E$
r = 10 : 10-bit resolution	E = 1 : $Error_{AREF}$ = $LSB_r / 2$	LSB_r = $V_{AREF} / 2^r$
r = 12 : 12-bit resolution	E = 2 : $Error_{AREF}$ = $LSB_r / 4$	

Note: The maximum voltage error ($Error_{AREF}$) at V_{AREF} caused by C_{AREF} is referenced to the allowed maximum input voltage at ANx ($V_{AINx} = V_{AREF}$). For input voltages at ANx smaller than V_{AREF} the additional in-accuracy at V_{AINx} is proportionally less than the value of $Error_{AREF}$ used in the example calculations. The real additional inaccuracy at V_{AINx} is:
$Error_{AREF\_real} = (V_{AINx} / V_{AREF}) * Error_{AREF}$ with the condition: $V_{AGND} \leq V_{AINx} \leq V_{AREF}$

Table 8 shows the minimum C_{AREF} values required for different values of A/D converter resolution, and the maximum allowed $ERROR_{AREF}$ at the reference voltage input V_{AREF}.

Table 8 C_{AREF} Minimum Value for different Conditions

A/D converter resolution	8bit	10bit	12bit
C_{AREF_MIN} ($ERROR_{AREF}$ = 1 LSB):	4 nF	15 nF	61 nF
C_{AREF_MIN} ($ERROR_{AREF}$ = 0.5 LSB):	8 nF	31 nF	123 nF
C_{AREF_MIN} ($ERROR_{AREF}$ = 0.25 LSB):	15 nF	61 nF	246 nF
C_{AREF_MIN} ($ERROR_{AREF}$ = 0.125 LSB):	31 nF	123 nF	492 nF

The condition ($C_{AREF} \geq 2^{r+E} * C_{AREFSW} / 2$) allows a free choice of the A/D converter clock, but the cycle time t_{CYCLE} has a direct influence on the accuracy of the conversion. The cycle time (total conversion time) has to be long enough to recharge the external capacitance C_{AREF} before the next charge-redistribution phase is started.

The external capacitance C_{AREF} has to be charged from the voltage reference. The minimum current, which is drawn from the voltage reference, is based on the charge that is necessary for a complete conversion. The charge Q_{CONV} for a complete charge-redistribution phase and a calibration phase is:

(16)

$$Q_{CONV} = C_{AREFSW} \cdot V_{AREF}$$

The current for the voltage reference depends on the minimum cycle time for a total conversion:

(17)

$$I_{AREF} = \frac{Q_{CONV}}{t_{CYCLE}}$$

The external resistance R_{REF} between the voltage reference V_{RF} and the input V_{AREF} of the A/D converter has a significant influence on the accuracy.

*Note: This resistor should be as small as possible because the continuous current I_{AREF} causes a voltage drop V_{ERROR} between the voltage reference V_{RF} and the reference voltage input V_{AREF} of the A/D converter (See **Figure 26**).*

(18)

$$V_{ERROR} = R_{REF} \cdot I_{AREF}$$

7.4.1 Calculation Example

The assumed values in this example are:

C_{AREFSW}	= 30 pF	t_S	= 0.6 µs	V_{RF}	= 5 V
R_{AREF}	= 1000 Ω	t_C	= 1.4 µs	r	= 12 (12-bit resolution)
E	= 1	$Error_{AREF}$	= 0.5 LSB_{12} = V_{RF} / 4096 / 2	$Error_{AREF}$	= 0.62 mV

The value for the external capacitance between V_{AREF} and V_{AGND} is:

$$C_{AREF} \geq 2^{r+E} * C_{AREFSW} / 2$$
$$C_{AREF} \geq 2^{12+1} * 30pF / 2$$
$$C_{AREF} \geq 123nF$$

Note: A typical recommendation for the value of the external capacitance is C_{AREF} = 220 nF. Using some µF, external capacitance C_{AREF} can significantly suppress noise on V_{AREF} and increase total accuracy.

Assuming $V_{AREF} = V_{RF}$, the minimum continuous current which has to be supplied by the voltage reference is:

$$I_{AREF} \geq C_{AREFSW} * V_{AREF} / t_{CYCLE}$$
$$I_{AREF} \geq 30\ pF * 5\ V / 2\ \mu s$$
$$I_{AREF} \geq 75\ \mu A$$

$$t_{CYCLE} = t_S + t_C$$
$$t_{CYCLE} = 0.6\ \mu s + 1.4\ \mu s$$
$$t_{CYCLE} = 2\ \mu s$$

The maximum allowed value for the resistor R_{REF} between voltage reference V_{RF} and input V_{AREF} of the A/D converter is:

$$R_{REF} \leq V_{ERROR} / I_{AREF}$$
$$R_{REF} \leq 0.61\ mV / 75\ \mu A$$
$$R_{REF} \leq 8.1\ \Omega\ @\ 12\ bit\ resolution\ and\ Error_{AREF} = 0.5\ LSB_{12}$$

Using 10 bit resolution:

$$R_{REF} \leq 32.5\ \Omega\ @\ 10\ bit\ resolution\ and\ Error_{AREF} = 0.5\ LSB_{10}$$

Note: In an overload condition it is possible that R_{REF} has to be increased, to limit the overload current to the specified values. If the value of R_{REF} exceeds the error limit of the system, an external diode between V_{AREF} and V_{DD} can reduce the overload current (See ***Figure 25 "External Voltage Reference" on Page 41****).*

Note: Depending on the implementation, in the best case there should be one input pin V_{AREF} per A/D converter. Some microcontrollers however may only have one V_{AREF} pin for several different A/D converters because of the pin limitations of the package being used. In this instance the external circuitry at pin V_{AREF} has to be selected after considering and summing up all individual A/D converter requirements.

7.5 Ratiometric Configuration

In a non-ratiometric configuration there is no relation between the voltage of the analog source and the reference voltage at pin V_{AREF}. Both the accuracy of the reference voltage and the accuracy of the analog source have an influence on the accuracy of the total A/D conversion system, because any changes in the supply voltage of the analog source results in a change at the analog input voltage (ANx) seen by the A/D converter. Since the voltage reference is independent from the analog source excitation, the A/D conversion result will reflect the changed excitation.

Figure 27 shows the principle of a ratiometric configuration. The same voltage reference source is used for the analog source excitation and the reference voltage input V_{AREF}. Therefore a given change in the analog source excitation causes the same change at the reference voltage V_{AREF}.

The A/D converter conversion result is the ratio of the analog input ANx, to the reference voltage V_{AREF}. Since both the analog input ANx and the reference voltage V_{AREF} are derived from the same voltage reference source, changes do not cause measurement errors. The A/D converter conversion result is therefore independent of variations in the analog source excitation or from variations in the reference voltage input V_{AREF}. A stable voltage reference is therefore not necessary to achieve an accurate measurement result.

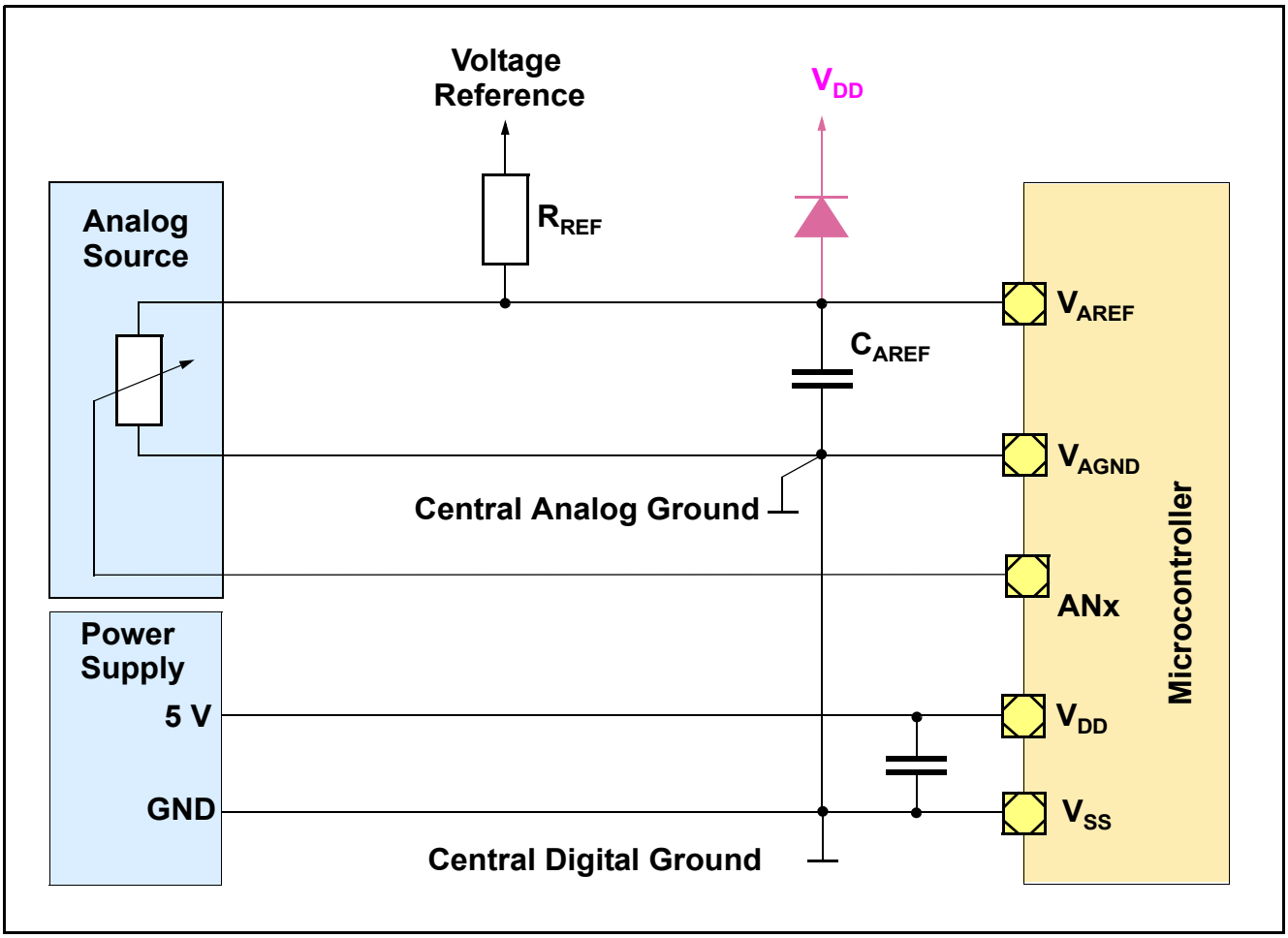

Figure 27 Ratiometric Configuration

8 Overload and Leakage Current

Both overload and leakage currents are specified in the Data Sheet of the selected microcontroller. Consideration of these currents can influence the design of the external components of the analog source. **Figure 28** is a simplified electrical model with ESD structure (clamp diodes) and leakage current of an analog input.

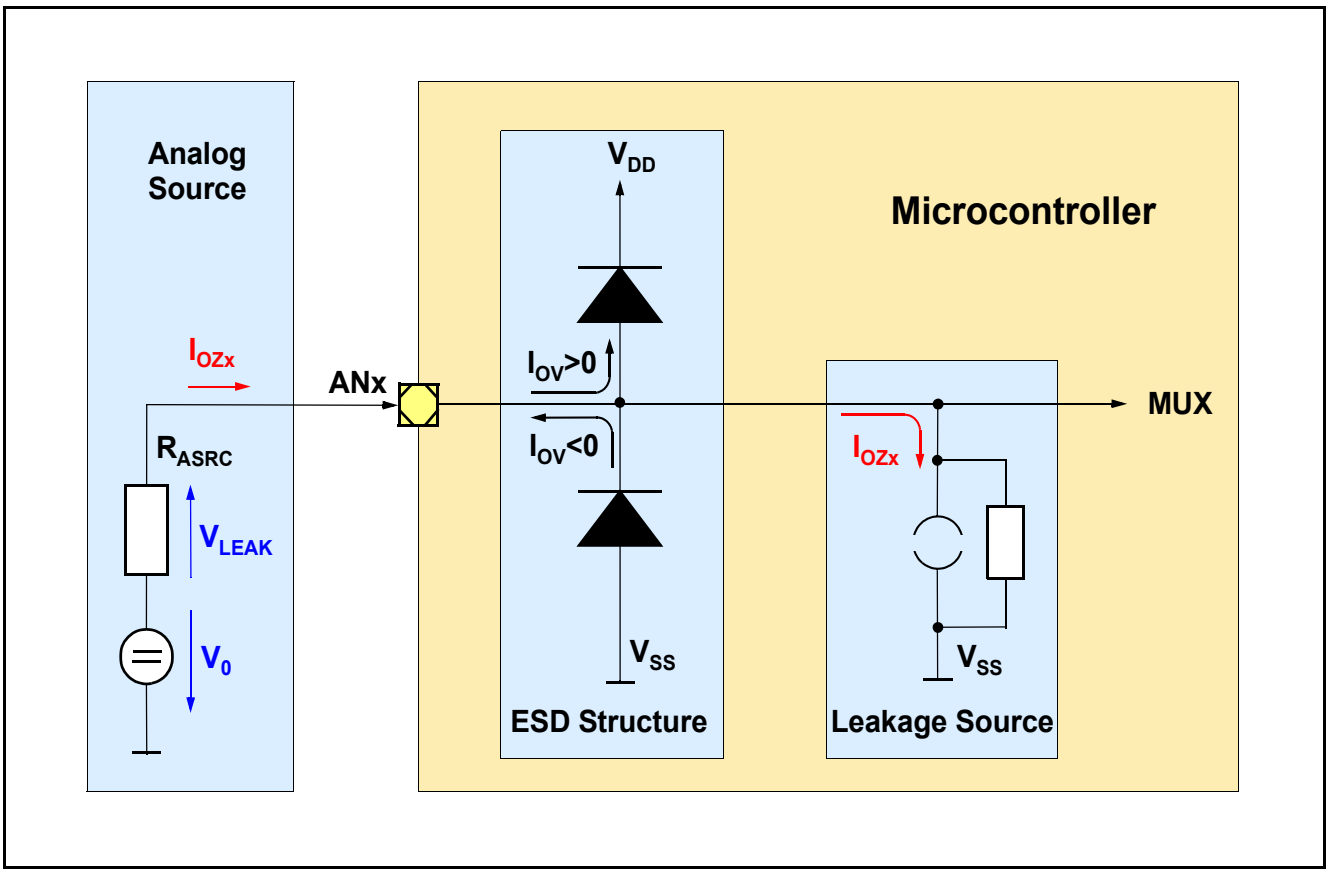

Figure 28 A/D Converter Input with ESD Structure and Leakage Source

*Note: The ESD structure of the reference voltage V_{AREF} and of the reference ground V_{AGND} is the same as shown in **Figure 28**.*

8.1 Leakage Current

The input leakage current is the sum of all currents which can flow into or out of an input pin caused by parasitic effects of the input structure (see **Figure 28**).

The maximum input leakage current of the A/D converter is specified in the 'DC Characteristics' section of the appropriate Data Sheet.

Note: The symbol for the input leakage current used in the Data Sheet is in most cases I_{OZx}.

The input leakage current has to be taken into account for the calculation of the maximum allowed error of the A/D converter result with reference to the analog source, because the resistance of the analog source R_{ASRC} and the input leakage current I_{OZx} can cause an additional error via the external 'leakage voltage' V_{LEAK}.

(19)

$$V_{LEAK} = I_{OZx} \cdot R_{ASRC}$$

The leakage voltage V_{LEAK} can cause an additional un-adjusted error AUE_{LEAK}.

(20)

$$AUE_{LEAK} = \frac{V_{LEAK}}{1LSBr}$$

8.1.1 Calculation Example

Assumed system values:

AUE_{LEAK}	= 0.5 LSB	Assumed maximum additional un-adjusted error caused by resistance of the analog source R_{ASRC} and leakage current
V_{AREF}	= 5 V	1 LSB_{12} = 1.22 mV
I_{OZx}	= |± 200 nA|	Maximum input leakage current

To calculate the allowed maximum resistance of the analog source R_{ASRC}:

R_{ASRC}	= V_{LEAK} / I_{OZx}
R_{ASRC}	= AUE_{LEAK} * 1LSB / I_{OZx}
R_{ASRC}	= 0.5 * 1.22 mV / 200 nA
R_{ASRC}	= 3050 Ω

Note: The Input Leakage Current can significantly reduce the total A/D conversion accuracy when the resistance of the analog source R_{ASC} has a high value.

8.2 Overload Current

An overload condition is not a normal operating condition. It occurs if the standard operating conditions are exceeded; i.e. the voltage on an A/D converter input pin V_{AINx} exceeds the specified range ($V_{AINx} > V_{DD} + 0.5$ V or $V_{AINx} < V_{SS} - 0.5$ V). The supply voltage must remain within the specified limits.

Where there is an overload condition on an A/D converter input pin, one of the clamp diodes becomes conductive:

- If $V_{AINx} > V_{DD} + 0.5$ V then the clamp diode connected to V_{DD} begins to conduct
- If $V_{AINx} < V_{SS} - 0.5$ V then the clamp diode connected to V_{SS} begins to conduct

(See **Figure 28 "A/D Converter Input with ESD Structure and Leakage Source" on Page 46**)

Notes

1. *The symbol for the overload current (also called injection current) used in the relevant microcontroller Data Sheet is in most cases I_{OV}.*
2. *The specified value of the A/D converter overload current depends on the device type. Please refer to the appropriate Data Sheet for the exact value.*
3. *The overload current has to be taken into account for the calculation of external resistors which protect the microcontroller inputs. These external resistors guarantee that, in case of a system error, the specified maximum value of the overload current will not be exceeded. The calculation also has to consider the specified absolute sum of input overload currents on all port pins or a pin group of the microcontroller, and especially the specified absolute sum of the A/D converter input.*

8.2.1 Overload Current and Absolute Maximum Ratings

The parameters of the **Absolute Maximum Ratings** are stress ratings only. The functional operation of the microcontroller is not guaranteed at these or other conditions above the 'operation conditions'.

Attention: Stresses above the absolute maximum ratings may cause permanent damage to the microcontroller. Exposing the microcontroller to absolute maximum rating conditions for extended periods may affect device reliability.

When the system is switched off, or in periods where it is not necessary to guarantee correct operation, the absolute maximum ratings are the fundamental information for the calculation of the input overload current, which may occur in case of a system error. In those instances the specified maximum overload current specified in the relevant Data Sheet may not be exceeded.

8.2.1.1 Calculation Example

Assumed system values:

V_{DD}	= 0 V	System supply voltage is off (worst case)
V_{Err_max}	= 14 V	Maximum voltage of the analog signal in case of a fatal system error
I_{OV_max}	= |±10 mA|	Maximum input leakage current (absolute maximum rating)

To calculate the minimum value for the external resistor R_P to protect an analog input pin for a short time overload condition:

$$R_{P\_min} = (V_{Err\_max} - V_{DD} - 0.5\ V) / I_{OV\_max}$$
$$R_{P\_min} = (14\ V - 0\ V - 0.5\ V) / 10\ mA$$
$$R_{P\_min} = 1350\ \Omega$$

8.2.2 Overload Current and Operating Conditions

The **Operating Conditions** must not be exceeded in order to ensure correct operation of the microcontroller.

The specified operating conditions allow a typical maximum overload current of I_{OV} = ±3 mA on any pin, and the absolute sum over input overload currents on all port pins is typically |50| mA.

The specified TUE of the A/D converter is guaranteed only if the specified absolute sum of input overload currents on all analog input pins is not exceeded. For the exact values, please refer to the appropriate Data Sheet.

8.2.2.1 Calculation Example

Assumed system values:

V_{DD}	= 4.5 V	Minimum system supply voltage during operating conditions (worst case)
V_{Err_max}	= 14 V	Maximum voltage of the analog signal in case of a fatal system error
I_{OV_max}	= |±3 mA|	Maximum of the overload current during operating conditions

To calculate the minimum value of the external resistor R_P to protect an analog input of the microcontroller and ensure correct operation:

$$R_{P\_min} = (V_{Err\_max} - V_{DD} - 0.5\ V) / I_{OV\_max}$$
$$R_{P\_min} = (14\ V - 4.5\ V - 0.5\ V) / 3mA$$
$$R_{P\_min} = 3000\ \Omega$$

Note: Overload current must be drained via ESD to V_{DD} line, otherwise V_{DD} could be charged up to 14V.

8.2.3 Coupling Factor

Depending on the A/D converter used, an overload current coupling factor for positive and negative overload currents (K_{OV}) is specified:

- K_{OVAP} is usually specified for positive overload currents
- K_{OVAN} is usually specified for negative overload currents

An overload current (I_{OV}) through a pin injects an error current ($|I_{INJ}| = |I_{OV}| * K_{OV}$) into the direct adjacent pins. This error current adds to that pin's leakage current (I_{OZ}).

The value of the error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is reversed from the polarity of the overload current that produces it.

The total leakage current through a pin is:

$$|I_{OZTOT}| = |I_{OZ}| + |I_{INJ}|$$
$$|I_{OZTOT}| = |I_{OZ}| + (|I_{OV}| * K_{OV})$$

The additional error current I_{INJ} distorts the analog input voltage V_{AINX} because of the additional voltage V_{LEAK} at R_{ASRC}. Details are shown in the following figure.

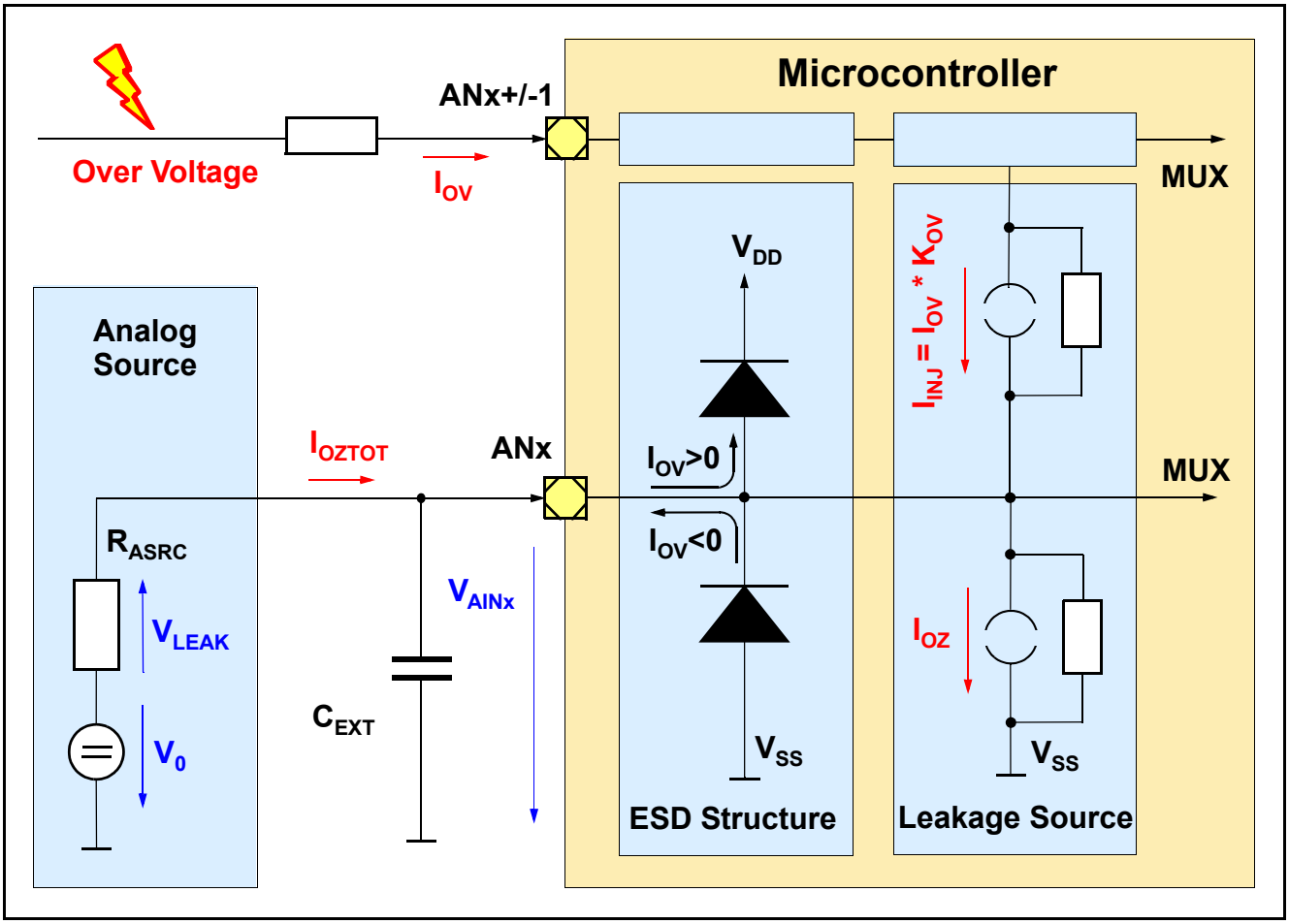

Figure 29 Relationship between Overload Current, Leakage Current and the Coupling Factor

8.2.3.1 Calculation Example

Assumed system values:

I_{OV}	= |±3 mA|	I_{OZ}	= |±200 nA|
K_{OVAP}	= 0.00001	K_{OVAN}	= 0.0001

Note: Details of the Overload Current, Leakage Current and Coupling Factor are described in the appropriate Data Sheet for each particular device.

To calculate the total leakage current:

I_{OZTOT_MAX}	= $\|I_{OZ}\| + (\|-I_{OV}\| * K_{OVAN})$	I_{OZTOT_MIN}	= $-\|I_{OZ}\| + (-\|I_{OV}\| * K_{OVAP})$
I_{OZTOT_MAX}	= 200 nA + 3 mA * 0.0001	I_{OZTOT_MIN}	= -200 nA - 3 mA * 0.00001
I_{OZTOT_MAX}	= 500 nA	I_{OZTOT_MIN}	= -230 nA

9 PCB and Design Considerations

This chapter is an introduction to mixed signal board design and offers a list of guidelines for optimum printed circuit board layout for microcontrollers with an on-chip A/D converter.

9.1 Component Placing

The guidelines for component placing are:

- Partition the board with all analog components grounded together in one area and all digital components in the other. Common power supply related components should be centrally located. An example is shown in **Figure 31 “Example for functional Partitioning” on Page 52**.
- Mixed signal components, including the microcontroller, should only bridge the partitions with analog pins in the analog area and digital pins in the digital area. Rotating the microcontroller can often make this task easier.

9.2 Power Supply

The guidelines for the power supply are:

- Place the analog power and voltage reference regulators over the analog plane.
- The digital power regulators should be over the digital plane.
- Analog power traces should be over the analog ground plane.
- Digital power traces should be over the digital ground plane.
- De-coupling capacitors should be close to the microcontroller pins, or positioned for the shortest connection to pins with wide traces to reduce impedance.
- If both large and small ceramic capacitors are recommended, position the small ceramic capacitor closest to the microcontroller pins.

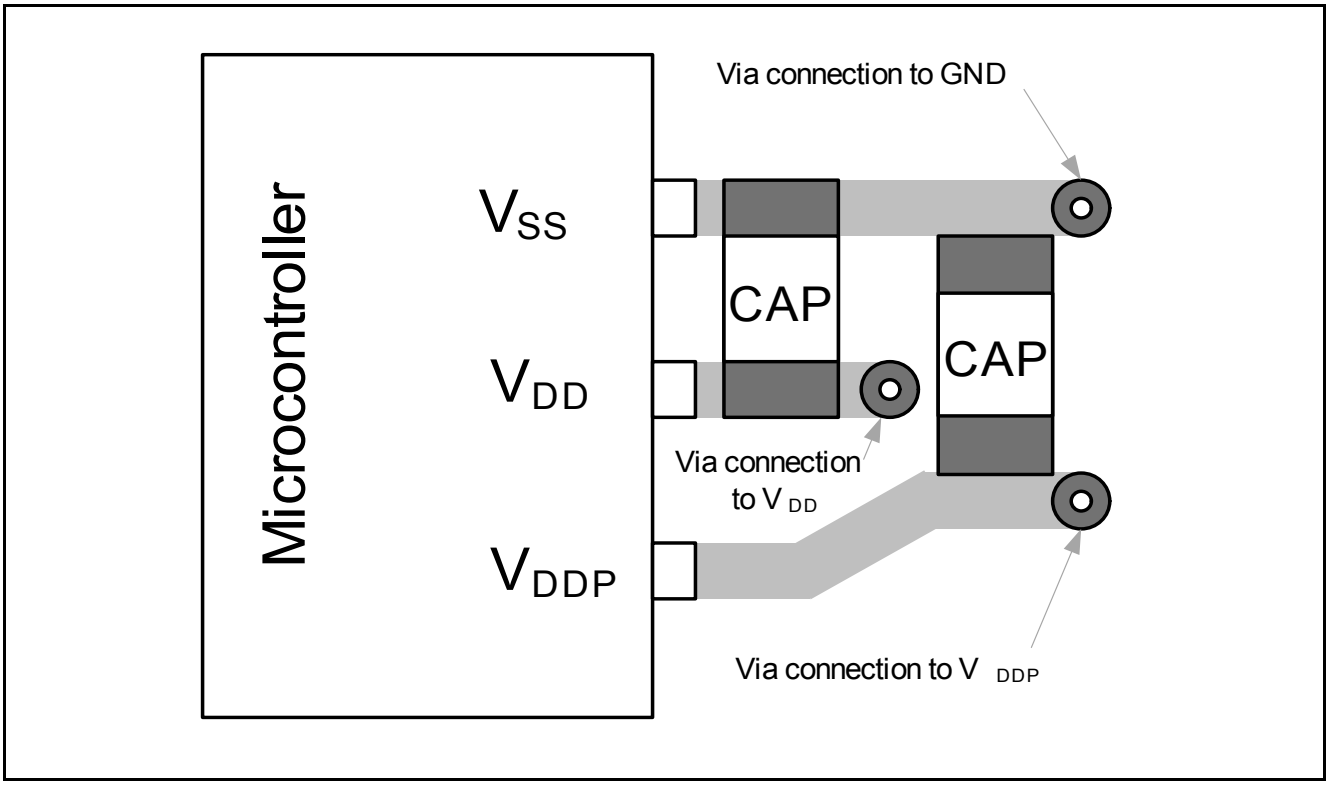

Figure 30 Example for Decoupling Capacitor Placing

9.3 Ground Planes

The guidelines for ground planes are:

- Have separate analog and digital ground planes on the same layer, separated by a gap, with the digital components over the digital ground plane and the analog components over the analog ground plane. An example for functional partitioning is shown in **Figure 31**.
- Analog and digital ground planes should only be connected at one point (in most cases). One of the best places is below the microcontroller. Have vias available in the board to allow alternative connection points.
- The connection of the analog and digital ground planes should be near to one of the following:
  - the power supply
  - the power supply connections to the board
  - the microcontroller
- For boards with more than two layers, **do not** overlap analog and digital related planes. Do not have a plane that crosses the gap between the analog ground plane and the digital ground plane region.

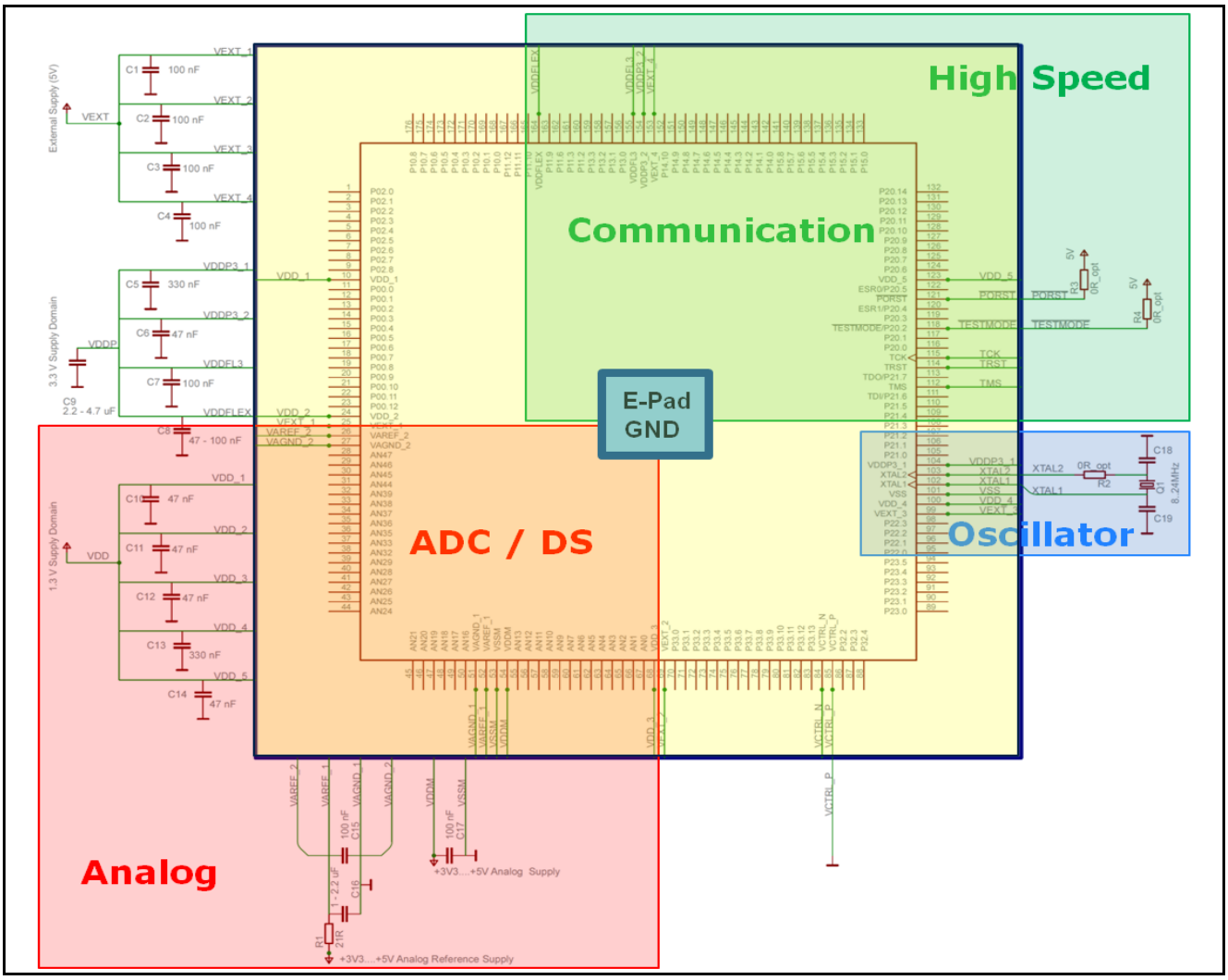

Figure 31 Example for functional Partitioning

9.4 Signal Lines

The guidelines for signal lines are:

- Analog signal traces should be over the analog ground plane.
- Digital signal traces should be over the digital ground plane.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane.
- Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane. These regions should not be left floating as this increases interference. The use of ground plane fill has been shown to reduce digital to analog coupling by up to 30 dB.

9.5 Clock Generation

The guidelines for clock generation are:

- Locate the quartz crystal, ceramic resonator or external oscillator as close as possible to the microcontroller.
- Keep digital signal traces, especially the clock signal, as far away from the analog input and voltage reference pins as possible.
- Avoid multiple oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D converter sampling clock.

10 Abbreviations

Abbreviation used in this document with an associated explanation.

Table 9 Abbreviations

Abbreviation	Explanation
ADC	Analog Digital Converter
ANx	Analog input x
AUE_{Leak}	Additional unadjusted error caused by the leakage current
C_{AINSW}	A/D converter switched input capacitance (internal C-net) $C_{AINWS} = C_{AINTOT} - C_{AINP}$
C_{AINSW_max}	Maximum value of the A/D converter switched input capacitance
C_{AINP}	A/D converter input pad capacitance
C_{AINTOT}	A/D converter input pad total capacitance
C_{AREF}	External capacitance connected to the reference voltage input V_{AREF}
C_{AREFP}	A/D converter input pad capacitance at V_{AREF}
C_{AREFSW}	A/D converter switched reference capacitance. $C_{AREFWS} = C_{AREFTOT} - C_{AREFP}$
$C_{AREFTOT}$	A/D converter total input pad capacitance at V_{AREF}
C_{EXT}	External capacitance connected to the analog input
C-Net	Internal A/D converter capacitor network.
$C_9 - C_0$	C-net for conversion (10-bit resolution).
$C_{7'} - C_{0'}$	C-net for calibration.
chn	Analog channel n
DNLE	Differential nonlinearity error
E	Variable for allowed Error to calculate C_{AREF}
$Error_{AINx}$	Maximum voltage difference between V_0 and V_{ANx} at the end of the sample time
$Error_{AREF}$	Maximum voltage error at V_{AREF} caused by C_{AREF}
ESD	Electrostatic discharge
f_{CPU}	CPU frequency
f_C	Cutoff frequency
f_{CYCLE}	Cycle frequency of sample events ($f_{CYCLE} = 1 / t_{CYCLEn}$)
f_{CYCLEn}	Cycle frequency of sample events at channel n
INLE	Integral nonlinearity error
I_{AREF}	Current of the voltage reference
I_{INJ}	Error current which is injected by an overload current to the direct adjacent pins
I_{OV}	Overload current
I_{OV_max}	Specified maximum rating of the overload current or Specified maximum of the overload current during operating conditions
I_{OZTOT}	Total input leakage current including Error current caused by overload current at adjacent pin
I_{OZTOT_MAX}	Maximum total input leakage current
I_{OZx}	Input leakage current
K_{OVA}	Analog overload coupling factor

Table 9 Abbreviations

Abbreviation	Explanation
K_{OVAN}	Analog overload coupling factor for negative overload current
K_{OVAP}	Analog overload coupling factor for positive overload current
LSB	Least significant bit (general)
LSB_r	Least significant bit referred to r-bit resolution ($LSB_r = V_{AREF} / 2^r$)
MSB	Most significant bit
r	Resolution of the A/D converter
R_{AIN}	Internal series resistance of the A/D converter
R_{ASRC}	Internal resistance of the analog source
R_{REF}	Resistance between voltage reference and V_{AREF} input
R_{AREF_EXT}	Internal resistance of the voltage reference
R_P	External resistor R_P to protect an analog input in case of an overload condition
R_{P_min}	Minimum value for the external resistor R_P
R_{ON}	Simulation: Sample switch R_{ON} resistance
t_C	Conversion time
t_{Cn}	Conversion time of analog channel n
t_{CYCLE}	Cycle time
t_{CYCLEn}	Cycle time of analog channel n
t_S	Sample time
t_1, t_2, t_3	Time constants for the different phases of a conversion
TUE	Total unadjusted error
V_{AREF}	Reference voltage input for the A/D converter
V_{AGND}	Reference ground for the A/D converter
V_{ANx}	Voltage at the analog input ANx
V_{CAINSW}	Voltage at the internal C-net
V_C (t)	Charge curve of C_{EXT} for a total cycle
V_C (t_{CYCLE})	Voltage of C_{EXT} at the end of a total cycle
V_{DD}	Supply voltage
V_{ERROR}	Voltage at R_{REF}
V_{ERR_max}	Maximum voltage of an analog signal in case of a fatal system error
V_{Leak}	Leakage voltage at R_{ASRC}
V_{LSB_12}	Simulation: Limitvoltage for the simulation plot ($V_{LSB\_12} = V_0 - 1LSB_{12}$)
$V_{PRECHARGE}$	Precharge voltage of the internal C-Net at start of sample time
V_R	Missing rest voltage of V_{AINx} at the end of a conversion cycle
V_{RF}	Voltage reference
V_{SS}	Digital GND
V_S(t)	Voltage curve during sample time
V_S(t_S)	Voltage at the end of sample time

Table 9 Abbreviations

Abbreviation	Explanation
V_0	Voltage of the analog source
V_Δ	Voltage drop at the beginning of the sample time

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