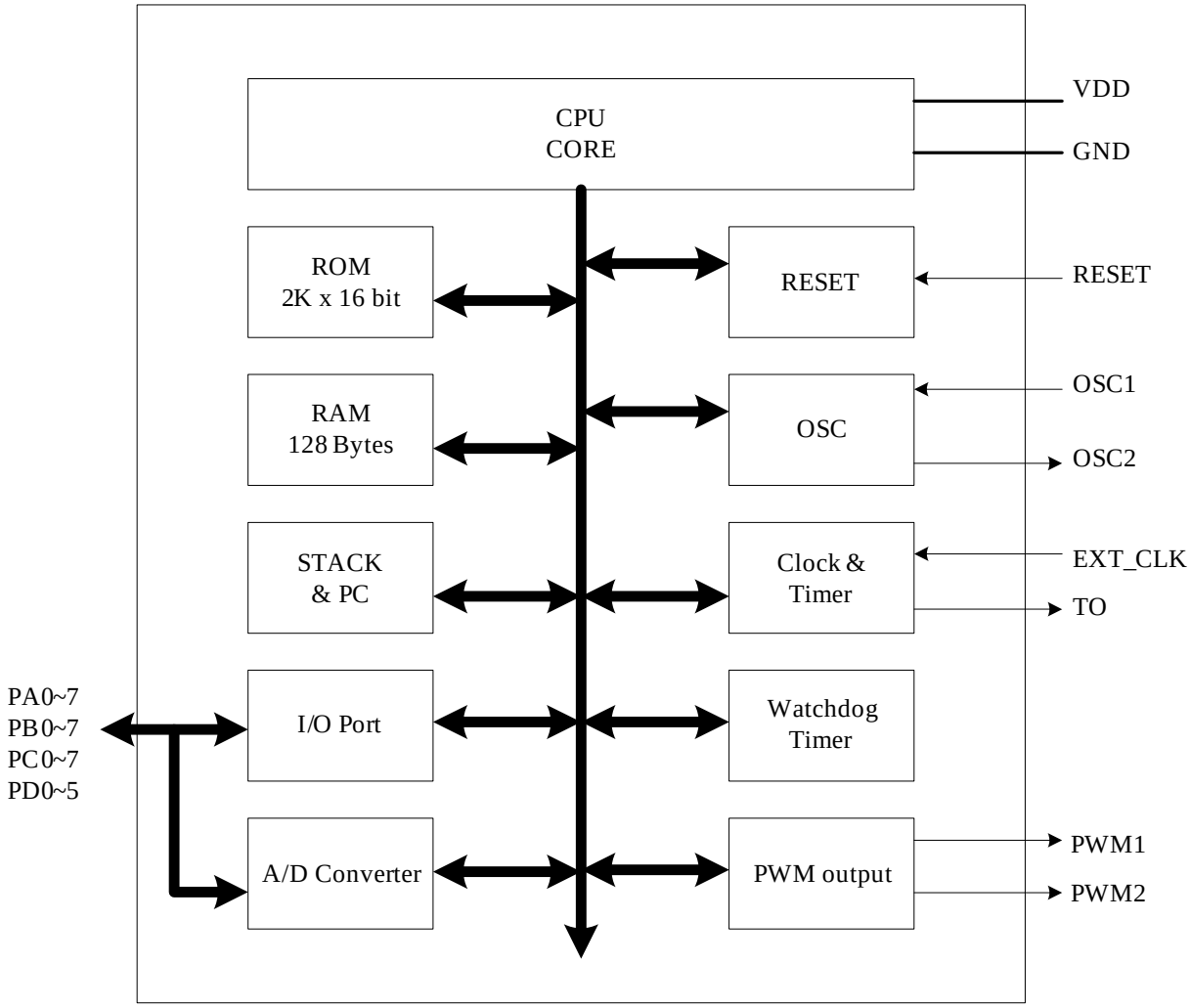
General Descrıptıon

The MK1841 is an 8 bit RISC high performance microcontroller with 15bit A/D converter. It is equipped with 2K word OTP(One Time Programmable) ROM, 128 Bytes RAM, Timer/Counter, Interrupt, LVR(Low Voltage Reset), I/O port, comparator and PWM output in a single chip.

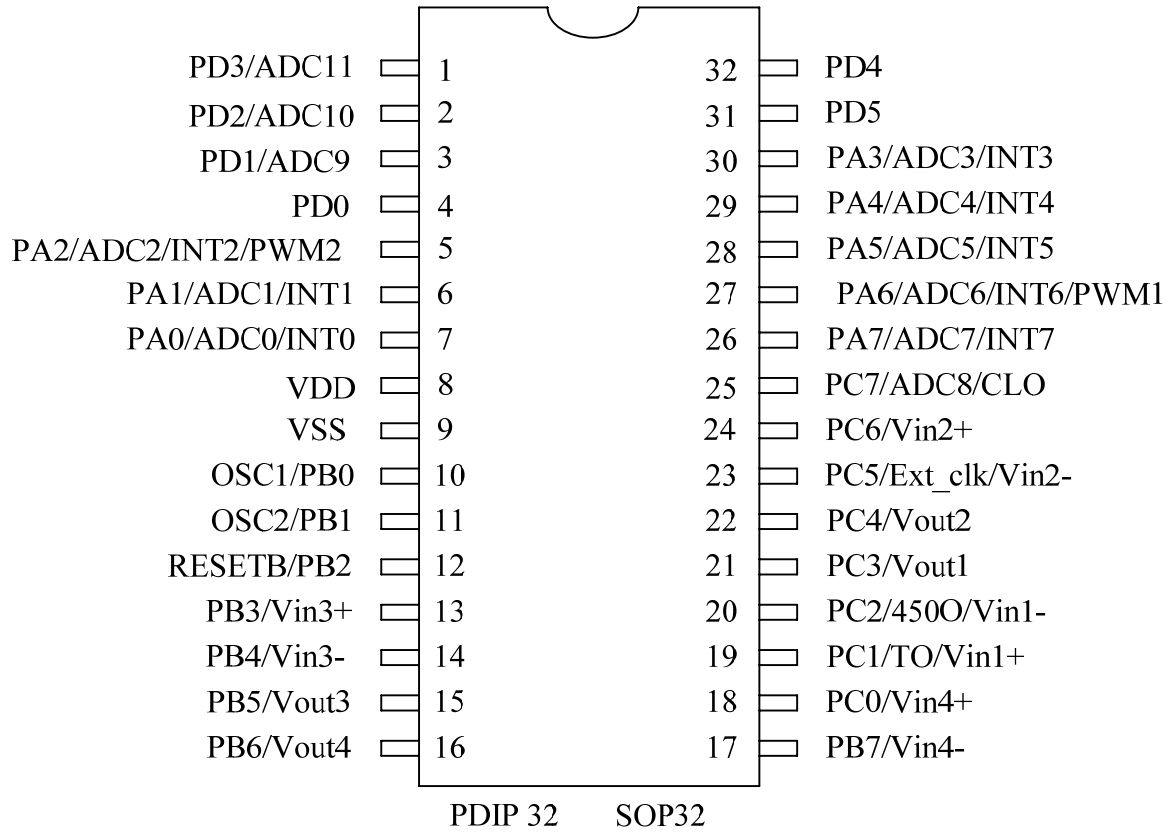
1. Feature

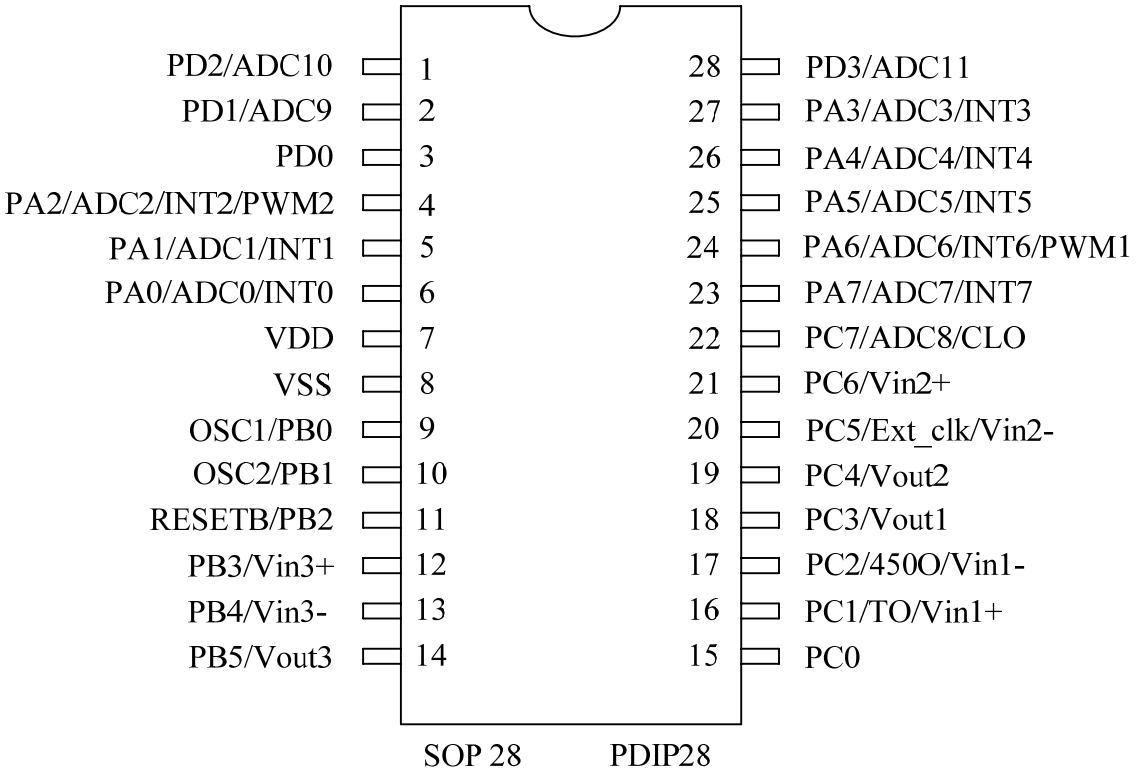
- ROM size: 2K x 16 bits
- RAM: 51 x 8 bits(Special Purpose Register) + 128 x 8 (General Purpose Register)
- STACK: 8 Levels
- One instruction is built by two systems clock.
- Reset mode:
  (a) Power-On reset
  (b) Low voltage reset
  (c) RESETB/PB2 (if be set as reset pin) input a negative pulse.
  (d) Watchdog timer count overflow reset
- Dual Clock Mode
  - External RC or Crystal oscillator
  - Internal 4MHZ RC oscillator
- Timer/counter: 5 units count up counter.
  - TM0: 16-bit Timer(up-counter)
  - TM1: 8-bit, PWM1(Period) & Timer
  - TM2: 8-bit, PWM1(Duty) & Timer
  - TM3: 8-bit, PWM2(Period) & Timer.
  - TM4: 8-bit, PWM2(Duty) & Timer.
  - TO : PWM2 cycle/2 output
- Watchdog Timer: On chip WDT is based on an internal RC oscillator (for WDT used only). Have 8 period can be selected. User can extend the WDT overflow period by using prescaler.
- Interrupt events:
  (a) External interrupt (PA7~PA0).
  (b) Internal timer/event counter interrupt (TM0~TM4, PWM1, PWM2).
  (c) ADC end of conversion interrupt
  (d) Comparators compare result activated interrupt.
- I/O port: 29 pins
- 4 Comparator sets which are shared pin with I/O port
- PWM: two channels with 8 bit x 8 bit resolution
- ADC: max 15-bit and 12 channels, at least 12-bit resolution. It can work at converter mode or compare mode by register setting
- Wake-up mode:
  - Port A (PA7~PA0) pin change wakeup -
  - WDT overflow
  - i_WDT overflow
- 500O :500KHZ Clock Out (Adjustable)
- CLO : System Clock Out
- Operating voltage range
  2.2V ~ 5.5V
- Operating temperature range
  -40 ℃ ~ + 85 ℃

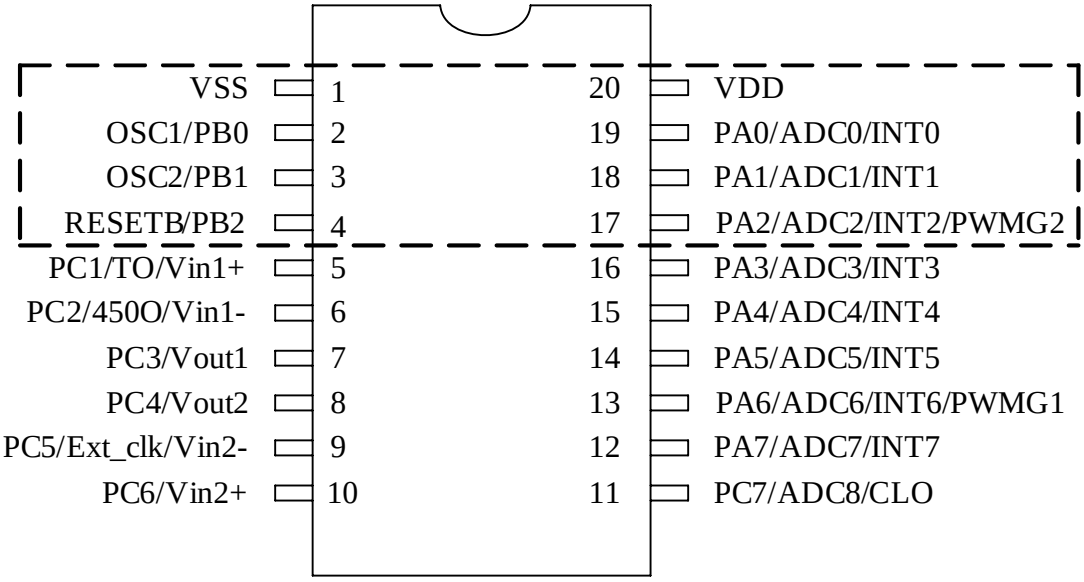
2. Block Diagram



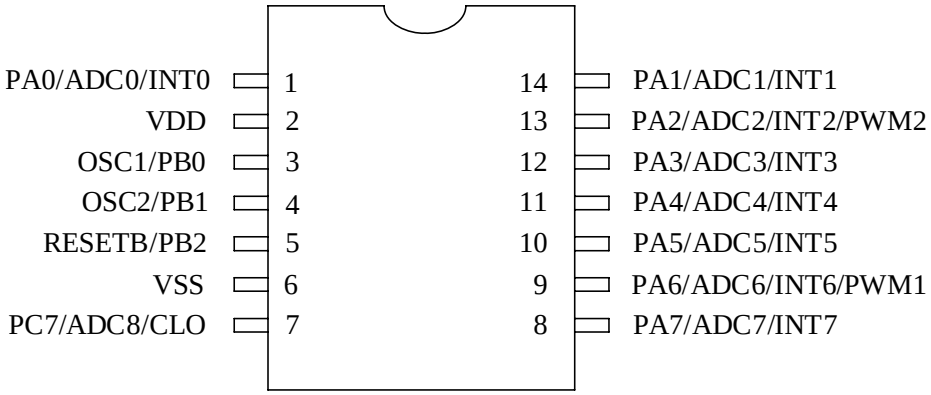
3. Pin Definition & Pad Assignment







PDIP 20/SOP 20



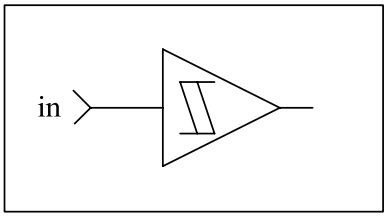
SOP 14

4. Pin Description

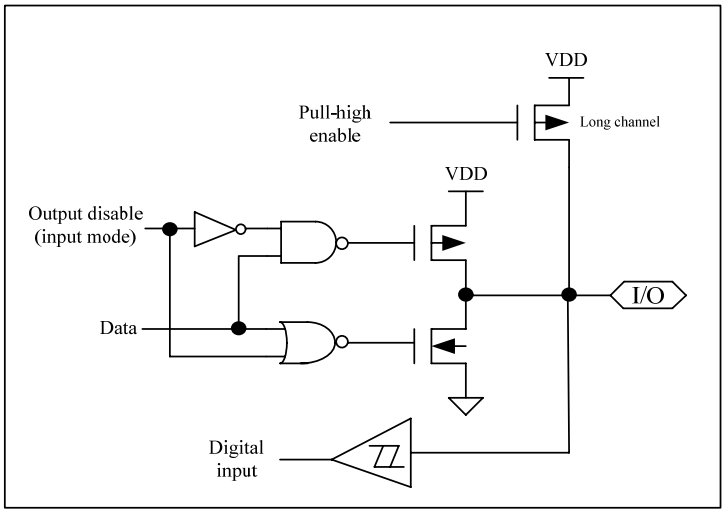
Pin name	I/O	Pin type	Description
PA0/ADC0/INT0 ~ PA1/ADC1/INT1 PA3/ADC3/INT3 ~ PA5/ADC5/INT5, PA7/ADC7/INT7	I/O	A	1. Bi-direction I/O port (Pull-up option with Input mode) 2. Wake-up on pin change (option) 3. External interrupt input (option) 4. A/D converter input
PA2/ADC2/INT2/PWM2 PA6/ADC6/INT6/PWM1	I/O	A	1. Bi-direction I/O port (Pull-up option with Input mode) 2. Wake-up on pin change (option) 3. External interrupt input (option) 4. A/D converter input 5.PWM1 & PWM2 output
OSC1/PB0	I, I/O	C	1. Bi-direction I/O port (Pull-up option with Input mode) 2. Oscillator input
OSC2/PB1	O,I/O	C	1. Bi-direction I/O port (Pull-up option with Input mode) 2. Oscillator output
RESETB/PB2	I	B	1. Input port 2. System reset pin
PB3/Vin3+ PB4/Vin3-	I/O	A	1. PB3~PB4 is Bi-direction I/O port (Pull-up option in Input mode) 2. Pin shared with comparator3 Vin3+,Vin3- . Pull-high resistor are disabled automatically in this mode
PB5/Vout3	I/O	E	1. PB5 is Bi-direction I/O port (Pull-up option in Input mode) 2 Pin shared with comparator3 Vout3 . Pull-high resistor are disabled automatically in this mode
PB6/Vout4	I/O	E	1. PB6 is Bi-direction I/O port (Pull-up option in Input mode) 2 Pin shared with comparator4 Vout4 . Pull-high resistor are disabled automatically in this mode
PB7/Vin4-	I/O	A	1. PB7 is Bi-direction I/O port (Pull-up option in Input mode) 2. Pin shared with comparator4 Vin4- . Pull-high resistor are disabled automatically in this mode
PC0/Vin4+	I/O	A	1. PC0 is Bi-direction I/O port (Pull-up option in Input mode) 2. Pin shared with comparator4 Vin4+ . Pull-high resistor are disabled automatically in this mode
PC1/TO/Vin1+ PC2/500O/Vin1-	I/O	A	3. PC1~PC2 is Bi-direction I/O port (Pull-up option in Input mode) 4. Pin shared with comparator1 Vin1+,Vin1- .

			5. If the comparator function is used, PC1~PC2 cannot be used Vin1+,Vin1- are analog input, Pull-high resistor are disabled automatically in this mode 6. TO(PWM2 interrupt/2) shared with PC1 7. 500O(500KHz clock out) shared with PC2 .
PC3/Vout1	I/O	E	1. PC3 is Bi-direction I/O port (Pull-up option in Input mode) 2 Pin shared with comparator1 Vout1 . Pull-high resistor are disabled automatically in this mode
PC4/Vout2	I/O	E	1. PC4 is Bi-direction I/O port (Pull-up option in Input mode) 2 Pin shared with comparator2 Vout2 . Pull-high resistor are disabled automatically in this mode
PC5/EXT_CLK/Vin2- PC6/Vin2+	I/O	A	1. PC5~PC6 is Bi-direction I/O port (Pull-up option in Input mode) 2. Pin shared comparator2 Vin2+,Vin2- . 3. If the comparator function is used, PC5~PC6 will be disable Vin2+,Vin2- are analog input, Pull-high resistor are disabled automatically in this mode 4. EXT_CLK (External clock input) shared with PC5
PC7/ADC8/CLO	I/O	A	1.Bi-direction I/O port (Pull-up option in Input mode) 2.A/D converter input 3.CLO (system clock out)shared with PC7.
PD0	I/O	D	1.Bi-direction I/O port (Pull-up option in Input mode)
PD1/ADC9~PD3/ADC11	I/O	A	1. Bi-direction I/O port (Pull-up option in Input mode) 2. A/D converter input
PD4~PD5	I/O	D	1.Bi-direction I/O port (Pull-up option in Input mode)
VDD	P		Power input
VSS	P		Ground input

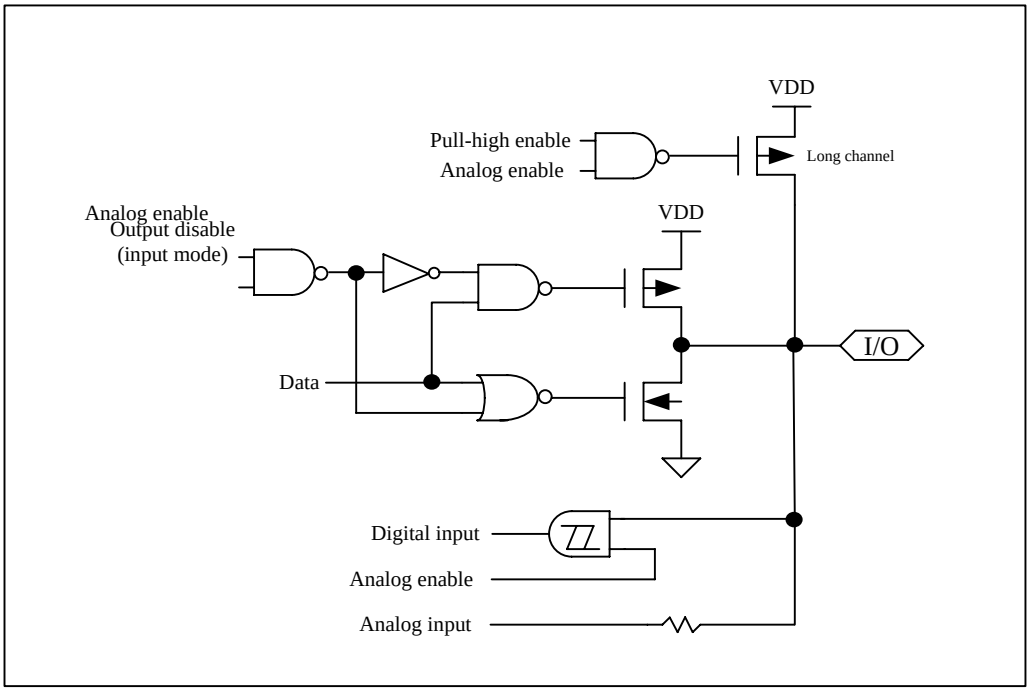
Pin Circuit



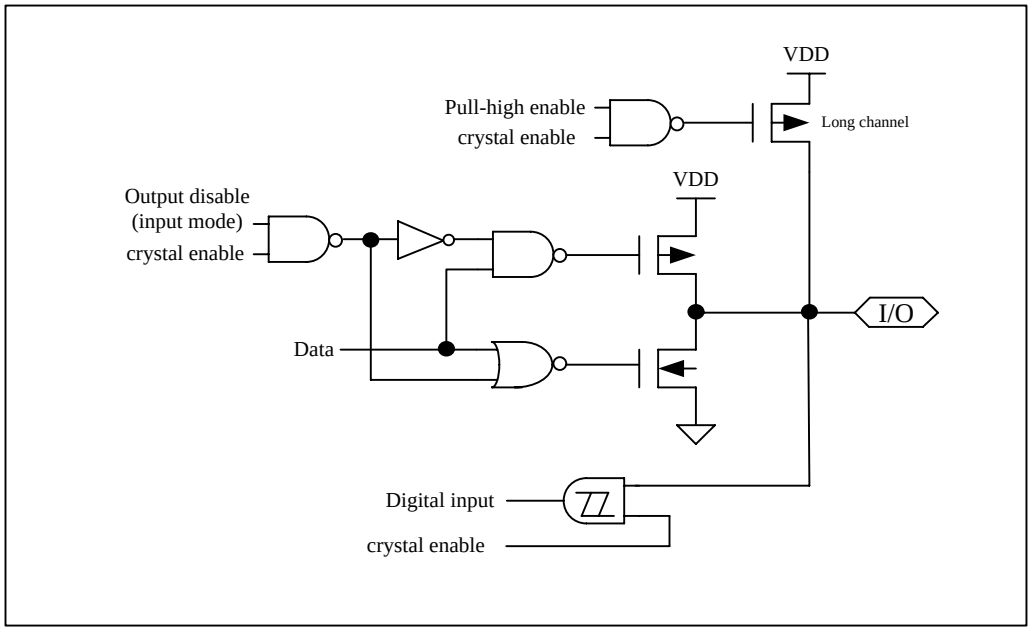
Pin circuit Type B



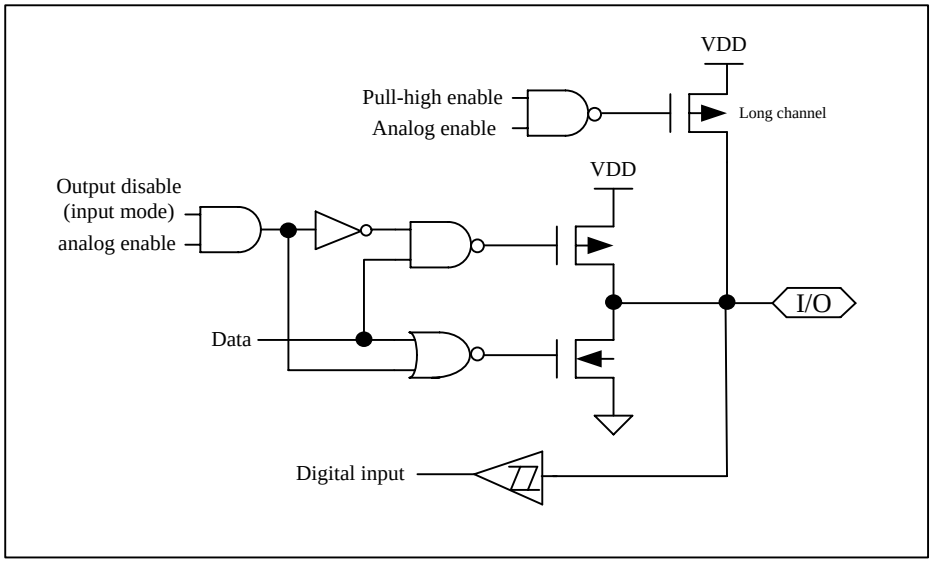
Pin circuit Type D



Pin circuit Type A



Pin circuit Type C



Pin circuit Type E

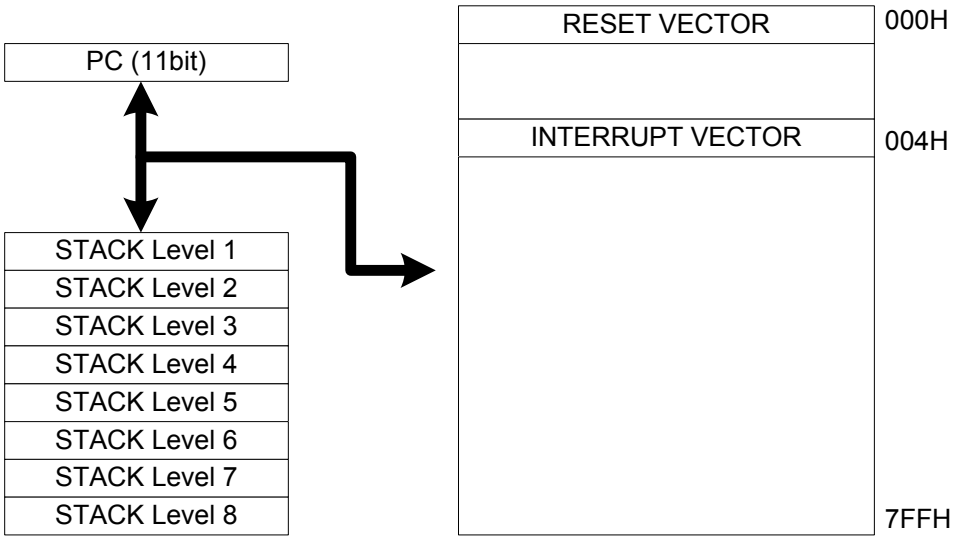
5. Memory Map

The BT1841 have two kinds of memory which are ROM (program memory) and RAM (data memory). The ROM is used to store the program, table and interrupt vectors. It is continuous 2048 X 16bits and don't need to switch bank. The RAM is 179(51+128) X 8 bits that include special function register and general-purpose RAM.

5.1 Program Memory (ROM)

Instruction and table are stored at this area. There is only one interrupt vector existed which means all the interrupt occurred would jump to the same vector. Programmer should use interrupt flag to judge what kind of interrupt is occurred. The program counter (PC) is 11 bit which can directly address all the 2048 x 16 location. Look-up table can be put at anywhere of ROM.

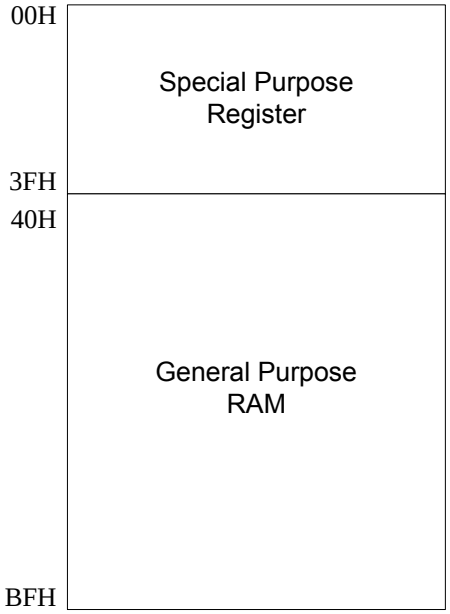
The RESET vector is located at 000H and Interrupt vector is at 004H. The map is as below:



5.2 Data Memory (RAM)

The total RAM volume are 179x8bits which includes two kinds of register group. One is 128×8 bits general purpose RAM, the other is special purpose register that are 51×8 bits. Every byte of special purpose register stored control's data or operation's data.

The data memory map is as below:



5.2.1 Special Purpose Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG_L		RST_DEF	LV1	LV0	WDTE	CPRT	INRC	FOSC1	FOSC0
CONFIG_H		ADJ6	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	RTCEN
INDF	$00	A7	A6	A5	A4	A3	A2	A1	A0
PCL	$01	A7	A6	A5	A4	A3	A2	A1	A0
PCH	$02	--	--	--	--	--	A10	A9	A8
STATUS	$03	--	--	--	$\overline{TO}$	$\overline{PD}$	Z	DC	C
FSR	$04	D7	D6	D5	D4	D3	D2	D1	D0
I/O PAD & Control									
Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_DIR	$05	IOA7	IOA6	IOA5	IOA4	IOA3	CA2	IOA1	IOA0
PA_DAT	$06	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
PB_DIR	$07	IOB7	IOB6	IOB5	IOB4	IOB3	--	IOB1	IOB0
PB_DAT	$08	DB7	DB6	DB5	DB4	DB3	--	DB1	DB0
PC_DIR	$09	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0
PC_DAT	$0A	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
PD_DIR	$0B	--	--	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0
PD_DAT	$0C	--	--	DD5	DD4	DD3	DD2	DD1	DD0
Timer 0: 16-bit Timer									

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_CTL	$10	TM0_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0
TM0L_LA	$11	D7	D6	D5	D4	D3	D2	D1	D0
TM0H_LA	$12	D7	D6	D5	D4	D3	D2	D1	D0
TM0L_CNT	$13	D7	D6	D5	D4	D3	D2	D1	D0
TM0H_CNT	$14	D7	D6	D5	D4	D3	D2	D1	D0

Timer 1: 8-bit, PWM (period) & Timer

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_CTL1	$15	TM1_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0
TM1_CTL2	$16	MOD	PWM1_OS	**	**	POS3	POS2	POS1	POS0
TM1_LA	$17	D7	D6	D5	D4	D3	D2	D1	D0
TM1_CNT	$18	D7	D6	D5	D4	D3	D2	D1	D0

Timer 2: 8-bit, PWM (duty) & Timer

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL	$19	TM2_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0
TM2_LA	$1A	D7	D6	D5	D4	D3	D2	D1	D0
TM2_CNT	$1B	D7	D6	D5	D4	D3	D2	D1	D0

Timer 3: 8 bit, PWM (period) & Timer

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL1	$1C	TM3_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0
TM3_CTL2	$1D	MOD	PWM2_OS	**	**	POS3	POS2	POS1	POS0
TM3_LA	$1E	D7	D6	D5	D4	D3	D2	D1	D0
TM3_CNT	$1F	D7	D6	D5	D4	D3	D2	D1	D0

Timer 4: 8 bit, PWM (duty) & Timer

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4_CTL	$20	TM4_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0
TM4_LA	$21	D7	D6	D5	D4	D3	D2	D1	D0
TM4_CNT	$22	D7	D6	D5	D4	D3	D2	D1	D0

IRQ

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM	$25	INTM	ADCM	PAM	TM4M	TM3M/PWM2M	TM2M	TM1M/PWM1M	TM0M
IRQF	$26	--	ADCF	PAF	TM4F	TM3F/PWM2F	TM2F	TM1F/PWM1F	TM0F
IRQM_1	$27	--	--	--	--	CMP4M	CMP3M	CMP2M	CMP1M
IRQF_1	$28	--	--	--	--	CMP4F	CMP3F	CMP2F	CMP1F

ADC control

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

AD_CTL1	$29	EN	--	MODE	--	CHSEL3	CHSEL2	CHSEL1	CHSEL0
AD_CTL2	$2A	RSUT	--	--	--	--	--	CKSEL1	CKSEL0
AD_CTL3	$2B	--	--	--	--	PISEL3	PISEL2	PISEL1	PISEL0
AD_DATL	$2C	D7	D6	D5	D4	D3	D2	D1	D0
AD_DATH	$2D	--	D14	D13	D12	D11	D10	D9	D8

Other

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP_CTL	$2F	--	--	--	--	CMP4_E	CMP3_E	CMP2_E	CMP1_E
FREQ_CTL	$30	S500O	500_PR1	500_PR0	--	--	500O_E	CLO_E	TO_E
PA_PLU	$31	UA7	UA6	UA5	UA4	UA3	UA2	UA1	UA0
PB_PLU	$32	UB7	UB6	UB5	UB4	UB3	--	UB1	UB0
PC_PLU	$33	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0
PD_PLU	$34	--	--	UD5	UD4	UD3	UD2	UD1	UD0
IO_CTL	$35	--	--	--	--	--	--	CK_FL	--
WAKEUP	$3A	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
WDT_CTL	$3D	WDTEN	i_WDT	i_STAB	--	--	PRE2	PRE1	PRE0
TAB_BNK	$3E	--	--	--	--	--	BNK2	BNK1	BNK0
SYS_CTL	$3F	CLKS	--	--	--	--	--	STPRC	STPOSC

<Note> "—" : mean no use.

"**" : mean is 0 (initial=0)

5.2.2 Configure Register

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG_L	RST_DEF	LV1	LV0	WDTE	CPRT	INRC	FOSC1	FOSC0
-	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CONFIG_H	ADJ6	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	EXT_CLK

- Bit15~9 (ADJ6~0): Used to calibrated internal RC oscillator.
- Bit8 (EXT_CLK): EXT_CLK input

  1: EXT_CLK (PC5) pin is timer source input & PC5 input.

  0: EXT_CLK (PC5) pin is normal I/O pin
- Bit7 (RST_DEF): RESETB pin define

  0: RESETB is normal input pin

  1: RESETB is system reset pin

- Bit6~5 (LV1~0): Set reset voltage level of Low Voltage Reset (LVR)

Bit6	Bit5	Detect voltage
LV1	LV0	
0	0	4V
0	1	Unimplemented
1	0	2.1V
1	1	Don't use

<Note> The power-down voltage may be influenced by process and temperature, so the listed voltage will have some tolerance.

- Bit4 (WDTE): Watchdog timer enable/disable

  0: WDT disable

  1: WDT enable

- Bit3 (CPRT): ROM Code Protection bit

  0: ON

  1: OFF

- Bit2~0 (INRC, FOSC1~0): OSC type and system clock select

Bit2	Bit1	Bit0	OSC Type	Resonance Frequency
INRC	FOSC1	FOSC0		
0	0	0	LS (low speed)	System clock=32~200KHz
0	0	1	NS (Normal speed)	System clock=200K~10MHz
0	1	0	HS (high speed)	System clock=10~20MHz
0	1	1	Dual RC clock: External RC & Internal RC	System clock=32K ~ 10MHz
1	0	0	LS &Internal RC	1. Dual clock mode LS & 4MHz 2. Initial system clock=4MHz
1	0	1	NS &Internal RC	1. Dual clock mode NS & 4MHz 2. Initial system clock=4MHz
1	1	0	HS & Internal RC	1. Dual clock mode HS & 4MHz 2. Initial system clock=4MHz
1	1	1	Internal RC	1. System clock=4MHz 2. OSC1 & OSC2 work as I/O ports

6. Function Descriptions

This device provide many functions that are Timer, WDT, PWM, ADC, Interrupt, Table location, Reset, Program Counter and STATUS register. We would like to describe in detail.

6.1 I/O Port

There are 4 I/O ports to input or output data, each port has different functions programmed by user. The port A can be used as external interrupt, ADC analog input or PWM output by register option. The port B can be used as system reset or external RC oscillator input function. The port C can be used as ADC analog input, 500KHZ output, system clock output or PWM output function. The port D can be used as ADC analog input.

6.1.1 Port A

There are 3 registers to set the 8 I/O ports which are PA_DIR, PA_DAT, PA_PLU. Each pin of Port A can be external interrupt input or normal I/O. To know how to set these pins as external interrupt, please refer to Chapter 6.7. PA2(PWM2).PA6 (PWM1) can be set as PWM output.

A. PA_DIR($05H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_DIR	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0

- Bit7~0 (IOA7~0): To define each pin is input port or output port
  - 0: Output.
  - 1: Input.

B. PA_DAT($06H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_DAT	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

- Bit7~0 (DA7~0): Data buffer

C. PA_PLU($31H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PA_PLU	UA7	UA6	UA5	UA4	UA3	UA2	UA1	UA0

- Bit7~0 (UA7~0): Pull up enables/disable
  - 0: Pull-up disable.
  - 1: Pull-up enable.

6.1.2 Port B

There are 3 registers to set the 7 I/O ports which are PB_DIR, PB_DAT, PB_PLU. Each pin of Port B can be set as normal I/O. User can set Pull up while Port B is set as input mode. PB2 (RESETB) can be set as system-reset (Low voltage reset) or single input pin by CONFIG_L register. Normally, PB0 (OSC1) and PB1 (OSC2) is external oscillator pin, only when internal RC mode is selected, PB0 and PB1 can be normal I/O pin.

A. PB_DIR($07H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_DIR	IOB7	IOB6	IOB5	IOB4	IOB3	--	IOB1	IOB0

- Bit7~0 (IOB7~0): To define each pin is input port or output port

  0: Output.

  1: Input.

<Note> Bit2: Input only and is set to be RESET or Input port at CONFIG_L bit 7..

B. PB_DAT($08H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_DAT	DB7	DB6	DB5	DB4	DB3	--	DB1	DB0

- Bit7~0 (DB7~0): Data buffer

C. PB_PLU($32H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PB_PLU	UB7	UB6	UB5	UB4	UB3	--	UB1	UB0

- Bit7~0 (UB7~0): Pull up enable/disable.

  0: Pull-up disable.

  1: Pull-up enable.

6.1.3 Port C

There are 3 registers to set the 8 I/O ports which are PC_DIR, PC_DAT, PC_PLU. PC5 (Ext_clk)) can be set as External clk input. User can set Pull up while PC7 ~ PC0 are set as input mode. Pin PC5 has multiple functions. User should define it at CONFIG_H bit 8 at first.

A. PC_DIR($09H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_DIR	IOC7	IOC6	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0

- Bit7 ~ 0: To define each pin is input port or output port

  0: Output.

  1: Input.

B. PC_DAT($0AH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_DAT	DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0

- Bit7 ~ 0 (DC7 ~ 0): Data buffer

C. PC_PLU($33H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC_PLU	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0

- Bit7 ~ 0 (UC7 ~ 0): Pull up enable/disable.

  0: Pull-up disable.

  1: Pull-up enable

6.1.4 Port D

There are 3 registers to set the 6 I/O ports which are PD_DIR, PD_DAT, PD_PLU. Each pin of Port A can be used as normal I/O or ADC analog input.

A. PD_DIR($0BH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_DIR	--	--	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0

- Bit6~0 (IOD6~0): To define each pin is input port or output port

  0: Output.

  1: Input.

B. PD_DAT($0CH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_DAT	--	--	DD5	DD4	DD3	DD2	DD1	DD0

- Bit7~0 (DD7~0): Data buffer

C. PD_PLU($34H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD_PLU	--	--	UD5	UD4	UD3	UD2	UD1	UD0

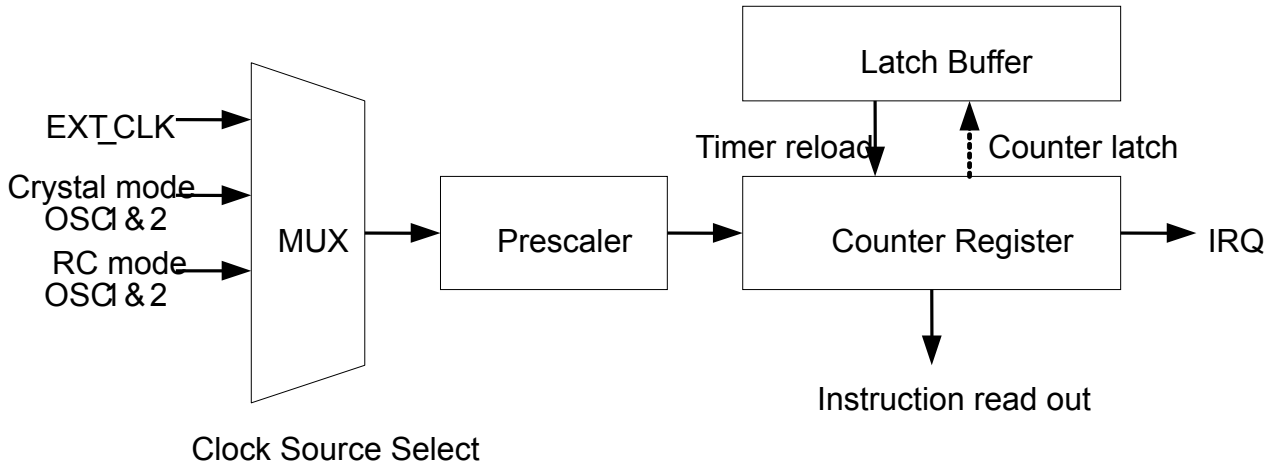
- Bit7~0 (UD7~0): Pull up enables/disable

  0: Pull-up disable.

  1: Pull-up enable.

6.2 Timer/Event Counter (TM0, TM1, TM2, TM3, TM4)

The BT1841 provide 5 up count timers/counters and 1 watchdog timer. Clock source of timers can be INRC, CRYSTAL or external clock by setting each timer control register. TM0 is a 16 bits timer, the others are 8 bit timer. All these timers have auto reload function, TM1/TM2 and TM3/TM4 can be cascaded to do PWM function. The detailed registers setting and block diagram are as below.



These timers have multiple functions which can be used as timer, PWM output waveform

6.2.1 TM0

TM0 is a 16 bit timer/counter. There are 5 registers to set its attributes.

A.TM0_CTL ($10H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0_CTL	TM0_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0

- Bit7 (TM0_EN): Timer0 enable/disable.

  0: TM0 disable.

  1: TM0 enable.

- Bit6 (WR_CNT): Latch buffer data write to counter register enable/disable.

  0: Latch buffer data write to counter register disable.

  1: Latch buffer data write to counter register enable

<Note> This bit is set only in the initial state of new timer/counter data to let latch buffer data write to counter register. When timer is overflow, the latch buffer data would auto reload into counter register. User doesn't need set again.

- Bit5~4 (SUR1~0): TM0 clock source selection bits

Bit5	Bit4	TM0 clock source
SUR1	SUR0	
0	0	EXT_CLK (PC5)
0	1	Crystal mode OSC1 or EXT_RC(In dual RC clock mode)
1	0	RC 4MHZ mode
1	1	Don't use

<Note> SUR1~0 define TM0 clock source.

Bit3 (EDGE): TM0 clock source edge control bit when the timer used as event counter

0: Increment when L→H on external clock

1: Increment when H→L on external clock

- Bit2~0 (PRE2~0): Set TM0 prescaler rate :

Bit2	Bit1	Bit0	TMR0 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

B. TM0L_LA/TM0H_LA and TM0L_CNT/TM0H_CNT Register ($11H, $12H, $13H, $14H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0L_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM0H_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM0L_CNT	D7	D6	D5	D4	D3	D2	D1	D0
TM0H_CNT	D7	D6	D5	D4	D3	D2	D1	D0

<Note1> Please don't write FFh data into TM0L_LA & TM0H_LA registers.

<Note2> TM0L_CNT & TM0H_CNT are read only registers

6.2.2 TM1 (or PWM1 period)

TM1 is an 8-bit timer/counter. There are 4 registers to set its attribute. The TM1 can be used as PWM1 period with TM2 to do PWM1 waveform.

A.TM1_CTL1 ($15H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_CTL1	TM1_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0

- Bit7 (TM1_EN): TM1(PWM1) enable/disable.
  0: TM1 disable.
  1: TM1 enable.
- Bit6 (WR_CNT): Latch buffer data write to counter register enable/disable.
  0: Latch buffer data write to counter register disable.
  1: Latch buffer data write to counter register enable

<Note> This bit is set only in the initial state of new timer/counter data to let latch buffer data write to counter register. When timer is overflow, the latch buffer data would auto reload into counter register. User doesn't need set again.

- Bit5~4 (SUR1~0): TM1 clock source selection bits

Bit5	Bit4	TM1/PWM1 clock source
SUR1	SUR0	
0	0	EXT_CLK (PC5)
0	1	Crystal mode OSC1 or EXT_RC(In dual RC clock mode)
1	0	RC 4MHZ mode
1	1	Don't use

- Bit3 (EDGE): TM1 clock source edge control bit when the timer used as event counter
  0: Increment when L→H on external clock
  1: Increment when H→L on external clock

- Bit2~0 (PRE2~0): Set TM1 prescaler rate

Bit2	Bit1	Bit0	TM1 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

B.TM1_CTL2 ($16H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_CTL2	MOD	PWM1_OS	**	**	POS3	POS2	POS1	POS0

- Bit7 (MOD) : TM1 can work in different mode, Timer, PWM mode which is setting as below table.

  0: TM1 work in timer mode

  1: TM1 work in PWM mode

- Bit6 (PWM1_OS): Set PWM1 output duty initial state

  0: Set the initial output state is H, this will change to L when TM2 timer overflow.

  1: Set the initial output state is L, this will change to H when TM2 timer overflow.

- Bit3~0 (POS3~0): PWM1 output pulse setting (Only active when TM1 work in PWM or PPG mode)

Bit3	Bit2	Bit1	Bit0	PWM1 pulse rate
POS3	POS2	POS1	POS0	
0	0	0	0	1:1
0	0	0	1	1:2
0	0	1	0	1:3
.	.	.	.	.
.	.	.	.	.
1	1	1	0	1:15
1	1	1	1	1:16

<Note> *In PWM mode*. 1:N means interrupt will be occurred after N PWM1 pulse.

C. TM1_LA & TM1_CNT ($17H, 18H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM1_CNT	D7	D6	D5	D4	D3	D2	D1	D0

<Note> TM1_CNT register is read only

6.2.3 TM2 (or PWM1 duty)

TM2 is an 8-bits timer/counter. There are 3 registers to set its attribute. TM2 can be used as PWM1 duty control with TM1 to do PWM1 waveform.

A.TM2_CTL ($19H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_CTL	TM2_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0

- Bit7 (TM2_EN): TM2 enable bit.

  0: TM2 disable.

  1: TM2 enable.

<Note> When TM1_CTL2 is set to PWM mode, this bit will be inhibited automatically. The TM2 became duty counter of PWM1 waveform.

- Bit6 (WR_CNT): Latch buffer data write to counter register enable/disable.

  0: Latch buffer data write to counter register disable.

  1: Latch buffer data write to counter register enable

<Note> This bit is set only in the initial state of new timer/counter data to let latch buffer data write to counter register. When timer is overflow, the latch buffer data would auto reload into counter register. User doesn't need set again.

- Bit5~4 (SUR1~0): TM2 clock source selection bits

Bit5	Bit4	TM2 clock source
SUR1	SUR0	
0	0	EXT_CLK (PC5)
0	1	Crystal mode OSC1 or EXT_RC(dual RC mode)
1	0	RC 4MHZ mode
1	1	Don't use

- Bit3 (EDGE): TM2 clock source edge control bit when the timer used as event counter

  0: Increment when L→H on external clock

  1: Increment when H→L on external clock

- Bit2~0 (PRE2~0): Prescaler assignment bit.

Bit2	Bit1	Bit0	TM2 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16

1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

B. TM2_LA & TM2_CNT ($1AH,1BH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM2_CNT	D7	D6	D5	D4	D3	D2	D1	D0

<Note> TM2_CNT register is read only

6.2.4 TM3 (or PWM2 period)

TM3 is an 8-bit timer/counter. There are 4 registers to set its attribute. The TM3 can be used as PWM2 period with TM4 to do PWM2 waveform.

A.TM3_CTL1 ($1CH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL1	TM3_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0

- Bit7 (TM3_EN): TM3 (PWM2) enable/disable.
  0: TM3 disable.
  1: TM3 enable.
- Bit6 (WR_CNT): Latch buffer data write to counter register enable/disable.
  0: Latch buffer data write to counter register disable.
  1: Latch buffer data write to counter register enable

<Note> This bit is set only in the initial state of new timer/counter data to let latch buffer data write to counter register. When timer is overflow, the latch buffer data would auto reload into counter register. User doesn't need set again.

- Bit5~4 (SUR1~0): TM3 clock source selection bits

Bit5	Bit4	TM3/PWM2 clock source
SUR1	SUR0	
0	0	EXT_CLK (PC5)
0	1	Crystal mode OSC1 or EXT_RC(dual RC mode)
1	0	RC 4MHZ mode
1	1	Don't use

- Bit3 (EDGE): TM3 clock source edge control bit when the timer used as event counter
  0: Increment when L→H on external clock
  1: Increment when H→L on external clock
- Bit2~0 (PRE2~0): Set TM3 prescaler rate

Bit2	Bit1	Bit0	TM3 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

B.TM3_CTL2 ($1DH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_CTL2	MOD	PWM2_OS	**	**	POS3	POS2	POS1	POS0

- Bit7 (MOD) : TM3 can work in different mode, Timer, PWM mode which is setting as below table

  0: TM3 work in timer mode

  1: TM3- work in PWM mode

- Bit6 (PWM2_OS): Set PWM2 output duty initial state

  0: Set the initial output state is H, this will change to L when TM4 timer overflow.

  1: Set the initial output state is L, this will change to H when TM4 timer overflow.

<Note> : " ** " bits are reserved for system and can not be set to "1".

- Bit3~0 (POS3~0): PWM2 output pulse setting (Only active when TM3 work in PWM mode)

Bit3	Bit2	Bit1	Bit0	PWM2 pulse rate
POS3	POS2	POS1	POS0	
0	0	0	0	1:1
0	0	0	1	1:2
0	0	1	0	1:3
.	.	.	.	.
.	.	.	.	.
1	1	1	0	1:15
1	1	1	1	1:16

<Note> *In PWM mode*. 1:N means interrupt will be occurred after N PWM2 pulse.

C. TM3_LA & TM3_CNT ($1EH, 1FH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM3_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM3_CNT	D7	D6	D5	D4	D3	D2	D1	D0

<Note> TM3_CNT register is read only

6.2.5 TM4 (or PWM2 duty)

TM4 is an 8-bits timer/counter. There are 3 registers to set its attribute. TM4 can be used as PWM2 duty control with TM3 to do PWM2 waveform.

A.TM4_CTL ($20H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4_CTL	TM4_EN	WR_CNT	SUR1	SUR0	EDGE	PRE2	PRE1	PRE0

- Bit7 (TM4_EN): TM4 enable bit.
  0: TM4 disable.
  1: TM4 enable.

<Note> When TM3_CTL2 is set to PWM2 mode, this bit will be inhibited automatically. The TM4 became duty counter of PWM2 waveform.

- Bit6 (WR_CNT): Latch buffer data write to counter register enable/disable.
  0: Latch buffer data write to counter register disable.
  1: Latch buffer data write to counter register enable

<Note> This bit is set only in the initial state of new timer/counter data to let latch buffer data write to counter register. When timer is overflow, the latch buffer data would auto reload into counter register. User doesn't need set again.

- Bit5~4 (SUR1~0): TM4 clock source selection bits

Bit5	Bit4	TM4 clock source
SUR1	SUR0	
0	0	EXT_CLK (PC5)
0	1	Crystal mode OSC1 or EXT_RC(dual RC mode)
1	0	RC 4MHZ mode
1	1	Don't use

- Bit3 (EDGE): TM4 clock source edge control bit when the timer used as event counter
  0: Increment when L→H on external clock
  1: Increment when H→L on external clock
- Bit2~0 (PRE2~0): Prescaler assignment bit.

Bit2	Bit1	Bit0	TM4 Prescaler rate
PRE2	PRE1	PRE0	
0	0	0	1:1
0	0	1	1:2
0	1	0	1:4
0	1	1	1:8
1	0	0	1:16
1	0	1	1:32
1	1	0	1:64
1	1	1	1:128

B. TM4_LA & TM4_CNT ($21H,$22H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM4_LA	D7	D6	D5	D4	D3	D2	D1	D0
TM4_CNT	D7	D6	D5	D4	D3	D2	D1	D0

<Note> TM4_CNT register is read only

C. CMP_CTL ($2FH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMP_CTL	--	--	--	--	CMP4_E	CMP3_E	CMP2_E	CMP1_E

- Bit3 (CMP4_E): Comparator 4 enable/disable .
  0: CMP4 disable.
  1: CMP4 enable.
- Bit2 (CMP3_E): Comparator 3 enable/disable .
  0: CMP3 disable.
  1: CMP3 enable.
- Bit1 (CMP2_E): Comparator 2 enable/disable .
  0: CMP2 disable.
  1: CMP2 enable.
- Bit0 (CMP1_E): Comparator 1 enable/disable .
  0: CMP1 disable.
  1: CMP1 enable.

6.3 PWM (Pulse Width Modulation)

PWM waveform is composed of TM1,3(period) and TM2,4(duty). These two timers can be used as general purpose timer or PWM waveform counter by setting register. The setting flow is as following example.

6.3.1 PWM

If timers are used as PWM, both of them are 8bit programmable duty and period. Each can generate pulse

width from 0.5us to 8,192ms when the system frequency is 4MHz. To set timers work in PWM mode, the register TM1_CTL2($16) or TM3_CTL2($1D) will be set to 1XX0XXXX(X means don't care). Please refer to below sample program and timing chart:

<Example> Timers work as PWM:

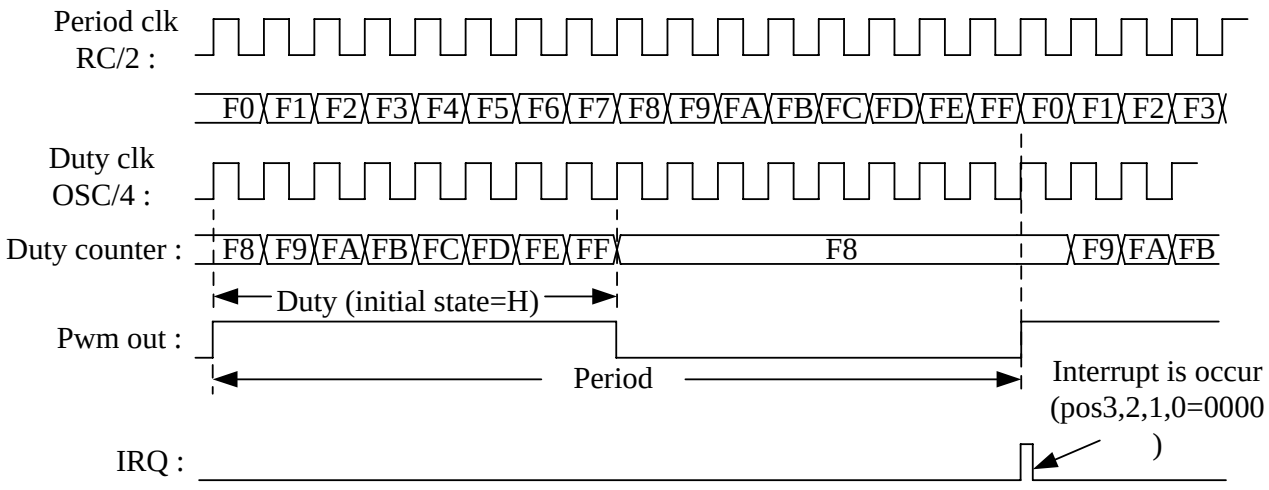
Set PWM period :

```
MOVLA     b01100001     ; set clk_source=RC, prescale=2
MOVAM     TM1_CTL1
MOVLA     b10000000
MOVAM     TM1_CTL2
MOVLA     F0H           ; set period counter value ( up count to FFH)
MOVAM     TM1_LA
```

Set PWM duty:

```
MOVLA     b01010010     ; set clk_source=OSC, prescale=4
MOVAM     TM2_CTL
MOVLA     F8H           ; set duty counter value (up count to FFH)
MOVAM     TM2_LA
BS        TM1_CTL1,b7   ; start PWM output
MOVLA     82H           ; enable INTM & PWM1 interrupt
MOVAM     IRQM
CLR       IRQF          ; clear interrupt flag
```

PWM Waveform



C.FREQ_CTL ($30H):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FREQ_CTL	S500O	500_PR1	500_PR0	--	--	500O_E	CLO_E	TO_E

- Bit7 (S500O) : Select clock source for 500khz Output .
  0: set 500Khz clock source = INRC (Init).
  1: set 500Khz clock source = OSC.
- Bit6,5 (S500_PR1, S500_PR0) : Prescaler assignment bit

Bit6	Bit5	500Khz prescaler
S500_PR1	S500_PR0	
0	0	1:2
0	1	1:4
1	0	1:8
1	1	1:16

- Bit2 (500O_E) : 500khz Output enable(pin shared with PC2) .
  0: set this pin is normal I/O pin
  1: set this pin is 500KHZ output
- Bit1 (CLO_E) : System clock output enable(pin shared with PC7).
  0: set this pin is normal I/O pin
  1: set this pin is system clock output.
- Bit0(TO_E) : The Timer out(TO) enable/disable (pin shared with PC1)
  0: Set this pin is PC1 normal I/O pin
  1: Set this pin is TO (Timer output pin, frequency is TM3 (PWM2) counter frequency /2)

<Note> Before TO signal output, the PC1 must set as output port.

6.5 WDT (Watchdog Timer)

WDT is a timer to prevent software from malfunction or jumping to an unknown location with unpredictable result. The source clock of WDT is an independent internal RC oscillator. This timer would be affected by temperature, voltage and different production lot.

A.WDT_CTL ($3DH):

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDT_CTL	WDTEN	i_WDT	i_STAB	--	--	PRE 2	PRE 1	PRE0

- Bit7 (WDTEN): Watchdog timer Enable bit
  0: WDT disable.
  1: WDT enable.
- Bit6 (i_WDT): i_WDT wakeup enable bit
  0: i_WDT disable.(init=disable)
  1: i_WDT enable.
- Bit5 (i_STAB): i_STAB wakeup times(in i_WDT mode) set bit

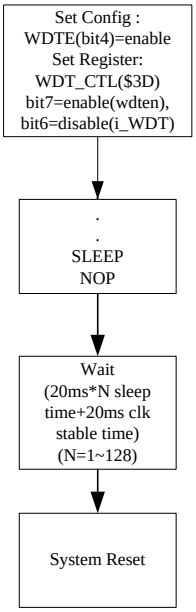
0: wakeup time=10ms(init)

1: wakeup time=5ms

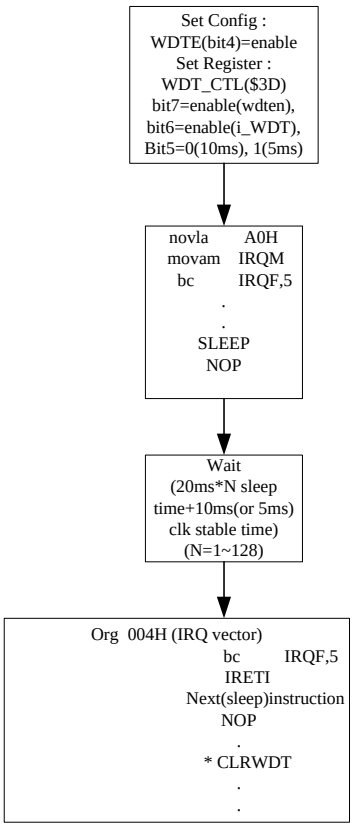
- Bit2~0 (PRE2~0): Set Prescaler rate. All the data are not accurate because it is RC OSC.

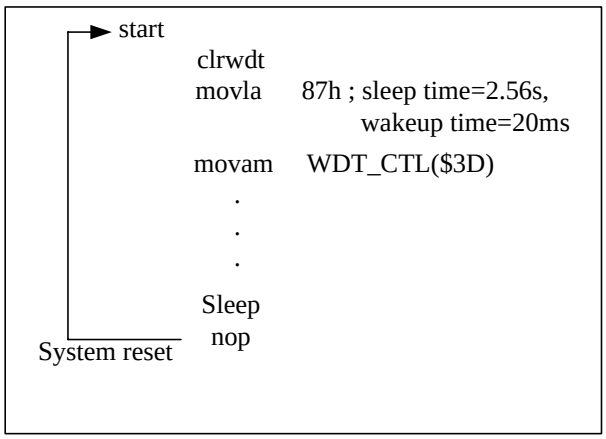
Bit2	Bit1	Bit0	WDT Prescaler rate
PRE2	PRE1	PRE1	
0	0	0	20mS
0	0	1	40mS
0	1	0	80mS
0	1	1	160mS
1	0	0	320mS
1	0	1	640mS
1	1	0	1.28S
1	1	1	2.56S

WDT-Wakeup :
(Watch-dog timer wake-up)

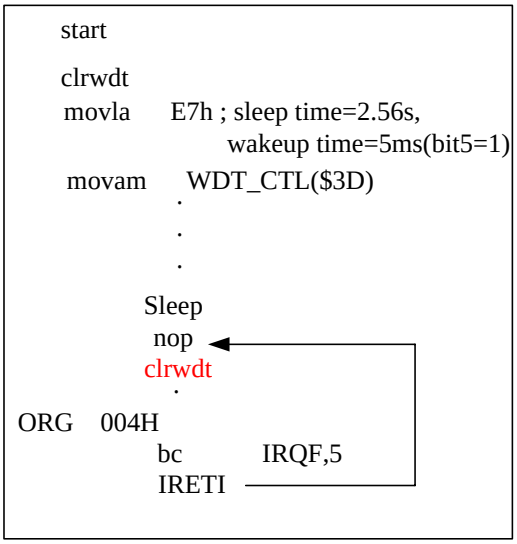


i_WDT-Wakeup :
(Internal watch-dog timer
wake-up)





*When wakeup must
CLRWDT, otherwise watch-
dog timer will keep operation



6.6 Reset

There are 4 events will cause reset which is listed as below. The power-down event will cause BT1841 reset and the detected voltage is according to the bit6~bit5 in the CONFIG register. This condition is used to protect chip in deficient power environment. The last two cases are called warm reset. The different reset events will affect registers and RAM. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset.

(1) Power-on reset.

(2) Low voltage reset (LVR).

(3) RESETB pin reset (input a negative pulse).

(4) WDT timer overflow reset.

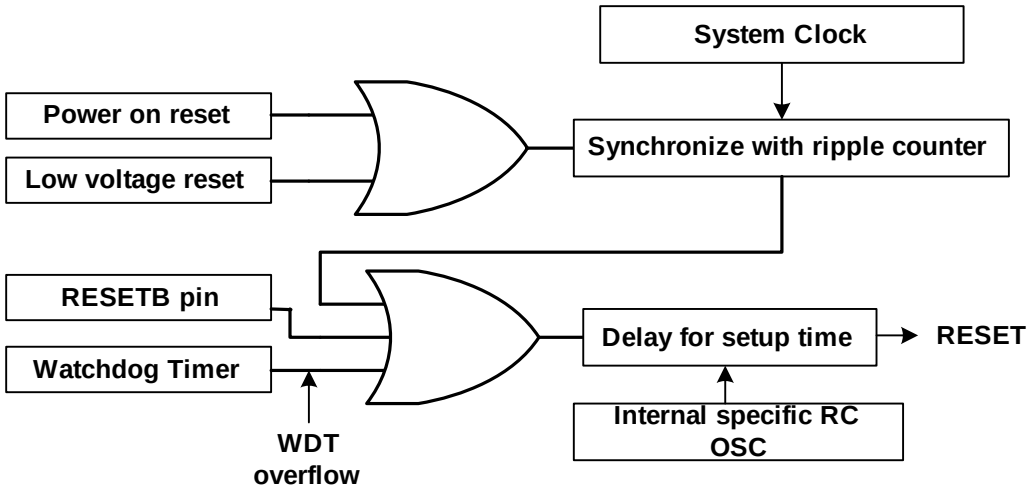


Figure: System Reset Block

<Note>: the watchdog setup time is approximately 20ms that will has some tolerance due to power voltage, process and temperature variations. Setup time is set by WDT_CTRL ($3DH).

The default value during different reset condition

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	pppp pppp
00H	INDF	0000 0000	0000 0000
01H	PCL	0000 0000	0000 0000
02H	PCH	- - - - -000	- - - - -000
03H	STATUS	0001 1xxx	0001 1xxx
04H	FSR	Xxxx xxxx	Pppp pppp
05H	PA_DIR	1111 1111	1111 1111
06H	PA_DAT	Xxxx xxxx	Pppp pppp
07H	PB_DIR	1111 1x11	1111 1x11
08H	PB_DAT	Xxxx xxxx	pppp pxpp

09H	PC_DIR	1111 1111	1111 1111
0AH	PC_DAT	Xxxx xxxx	pppp ppxp
0BH	PD_DIR	XX11 1111	XX11 1111
0CH	PD_DAT	Xxxx xxxx	xxpp pppp
10H	TM0_CTL	0000 0000	0000 0000
11H	TM0L_LA (Don't write FF)	0000 0000	0000 0000
12H	TM0H_LA (Don't write FF)	0000 0000	0000 0000
13H	TM0L_DAT (Read only)	1111 1111	1111 1111
14H	TM0H_ DAT (Read only)	1111 1111	1111 1111
15H	TM1_CTL1	0000 0000	0000 0000
16H	TM1_CTL2	0000 0000	0000 0000
17H	TM1_LA (Don't write FF)	0000 0000	0000 0000
18H	TM1_DAT (Read only)	1111 1111	1111 1111
19H	TM2_CTL	0000 0000	0000 0000
1AH	TM2_LA (Don't write FF)	0000 0000	0000 0000
1BH	TM2_DAT (Read only)	1111 1111	1111 1111
1CH	TM3_CTL1	0000 0000	0000 0000
1DH	TM3_CTL2	0000 0000	0000 0000
1EH	TM3_LA (Don't write FF)	0000 0000	0000 0000
1FH	TM3_DAT (Read only)	1111 1111	1111 1111
20H	TM4_CTL	0000 0000	0000 0000
21H	TM4_LA (Don't write FF)	0000 0000	0000 0000
22H	TM4_DAT (Read only)	1111 1111	1111 1111
25H	IRQM	0000 0000	0000 0000
26H	IRQF	x000 0000	x000 0000
27H	IRQM_1	xxxx 0000	xxxx 0000
28H	IRQF_1	xxxx 0000	xxxx 0000
29H	AD_CTL1	0x0x 0000	0x0x 0000
2AH	AD_CTL2	0xxx xx00	0xxx xx00
2BH	AD_CTL3	xxxx 0000	xxxx 0000
2CH	AD_DATL	0000 0000	0000 0000
2DH	AD_DATH	X000 0000	X000 0000
2FH	CMP_CTL	xxxx 0000	xxxx 0000
30H	FREQ_CTL	000x x000	000x x000
31H	PA_PLU	0000 0000	0000 0000
32H	PB_PLU	0000 0000	0000 0000

33H	**PC_PLU**	**0000 0000**	**0000 0000**
34H	**PD_PLU**	**Xx00 0000**	**Xx00 0000**
35H	**IO_CTL**	**Xxxx 0000**	**Xxxx 0000**
3AH	**WAKEUP**	**0000 0000**	**0000 0000**
3DH	**WDT_CTL**	**1xxx x111**	**1xxx x111**
3EH	**TAB_BNK**	**Xxxx x000**	**Xxxx x000**
3FH	**SYS_CTL**	**0xxx xx00**	**0xxx xx00**

X: unknown; **?: value depends on condition ;**

P: previous data; **-:unimplemented and read as"0".**

6.7 Interrupt

The BT1841 provides 7 external interrupt (PA0~7), three internal timer/event counter interrupt and an A/D converter interrupts. IRQM and IRQF registers are used to control or declare request state of all interrupts. The external interrupt is triggered by pin changed of PA0~7 and the related interrupt request flag (PAF; bit5 of IRQF) will be set. The A/D converter interrupt is initialized by setting the A/D converter request flag (ADCF; bit 6 of IRQF),interrupt is occurred when end of A/D conversion.

IRQM is used to enable/disable interrupt and IRQF is used to indicate which interrupt is occurred. If the specific IRQM doesn't enable at first then the hardware interrupt would not occurred. But the IRQF will response the status no matter how IRQM enable or not. For example, user enable TM1 to start counting. If IRQM bit 1 is enabled, the hardware interrupt would generate when timer overflow and IRQF bit 1 will be set. At the same time, program will jump to interrupt vector. User should clear IRQF in interrupt service routine, otherwise the interrupt would not generate again. Another condition is if IRQM bit 1 is disabled, the interrupt would not generate when timer overflow, but IRQF bit 1 still will be set. There is no hardware interrupt occurred and program would not jump to interrupt vector.

A. IRQM ($25H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM	**INTM**	**ADCM**	**PAM**	**TM4M**	**TM3M/PWM2M**	**TM2M**	**TM1M/PWM1M**	**TM0M**

- Bit7 (INTM): Global enable bit.
  0: Disable all interrupts mask.
  1: Enable all interrupt mask

<Note> When interrupt is serving, the INTM will reset to "0" to prevent the other interrupt happen. After being served, the IRETI instruction will set INTM as '1' automatically.

- Bit6 (ADCM): ADC end of conversion (EOC) interrupt enable:
  0: Disable Interrupt
  1: Enable Interrupt
- Bit5 (PAM): PA interrupt enable.
  0: Disable Interrupt

1: Enable Interrupt

- Bit4 (TM4M): TM4 interrupt enable
  0: Disable Interrupt
  1: Enable Interrupt
- Bit3 (TM3M/PWM2M): TM3/PWM2 interrupt enable
  0: Disable Interrupt
  1: Enable Interrupt
- Bit2 (TM2M): TM2 interrupt enable
  0: Disable Interrupt
  1: Enable Interrupt
- Bit1 (TM1M/PWM1M): TM1/PWM1 interrupt enable
  0: Disable Interrupt
  1: Enable Interrupt
- Bit0 (TM0M): TM0 interrupt enable
  0: Disable Interrupt
  1: Enable Interrupt

B. IRQF ($26H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF	--	ADCF	PAF	TM4F	TM3F/PWM2F	TM2F	TM1F/PWM1F	TM0F

- Bit6 (ADCF): ADC end of conversion interrupt request flag:
  0: End of conversion interrupt request off
  1: End of conversion interrupt request on
- Bit5 (PAF): PA0~7 Interrupt request flag:
  0: PA interrupt request off
  1: PA interrupt request on
- Bit4 (TM4F): TM4 Interrupt request flag:
  0: TM4 interrupt request off
  1: TM4 interrupt request on
- Bit3 (TM3F/PWM2F): TM3/PWM2 Interrupt request flag
  0: TM3/PWM2 overflow interrupt request off
  1: TM3/PWM2 overflow interrupt request on
- Bit2 (TM2F): TM2 interrupt request flag
  0: TM2 overflow interrupt request off
  1: TM2 overflow interrupt request on
- Bit1 (TM1F/PWM1F): TM1/PWM1 Interrupt flag
  0: TM1/PWM1 overflow or PWM1 interrupt request off

1: TM1/PWM1 overflow or PWM1 interrupt request on

- Bit0 (TM0F): TM0 interrupt request flag

  0: TM0 overflow interrupt request off

  1: TM0 overflow interrupt request on

C. IRQM_1 ($27H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQM_1	--	--	--	--	CMP4M	CMP3M	CMP2M	CMP1M

- Bit7 : Don't Use

  IRQM_1 global mask use the IRQM($25) bit7 (INTM).

<Note> When interrupt is serving, the INTM will reset to "0" to prevent the other interrupt happen. After being served, the IRETI instruction will set INTM as '1' automatically.

- Bit3 (CMP4M): Comparator4 interrupt enable:

  0: Disable Interrupt

  1: Enable Interrupt

- Bit2 (CMP3M): Comparator3 interrupt enable.

  0: Disable Interrupt

  1: Enable Interrupt

- Bit1 (CMP2M): Comparator2 interrupt enable:

  0: Disable Interrupt

  1: Enable Interrupt

- Bit0 (CMP1M): Comparator1 interrupt enable.

  0: Disable Interrupt

  1: Enable Interrupt

D. IRQF_1 ($28H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQF_1	--	--	--	--	CMP4F	CMP3F	CMP2F	CMP1F

- Bit3 (CMP4F): Compartaor4 interrupt request flag:

  0: Compartaor4 interrupt request off

  1: Compartaor4 interrupt request on

- Bit2 (CMP3F): Compartaor3 Interrupt request flag:

  0: Compartaor3 interrupt request off

  1: Compartaor3 interrupt request on

- Bit1 (CMP2F): Compartaor2 Interrupt request flag:

  0: Compartaor2 interrupt request off

  1: Compartaor2 interrupt request on

- Bit0 (CMP1F): Compartaor1 Interrupt request flag

  0: Compartaor1 interrupt request off

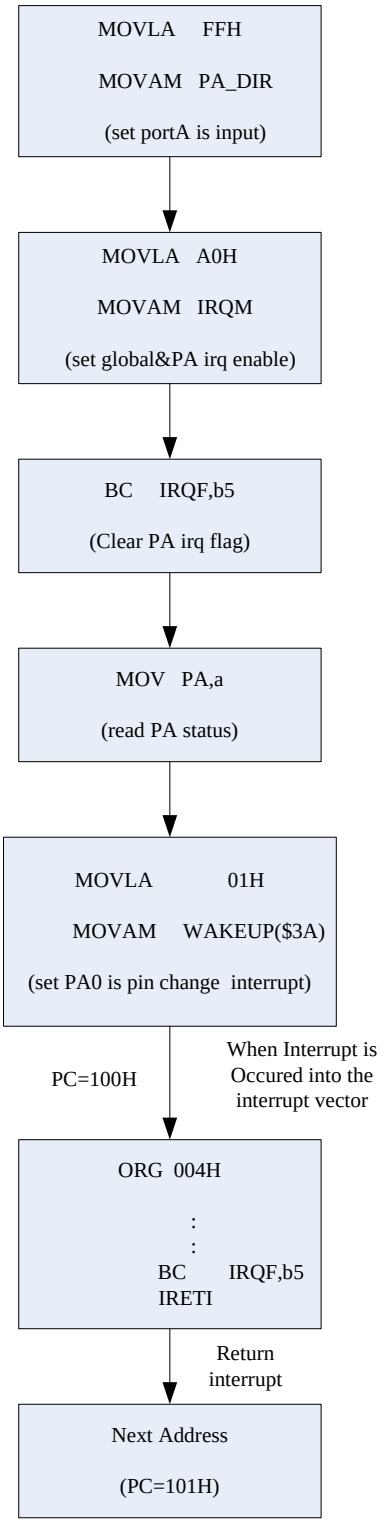
  1: Compartaor1 interrupt request on

6.7.1 External interrupt / Wake up function

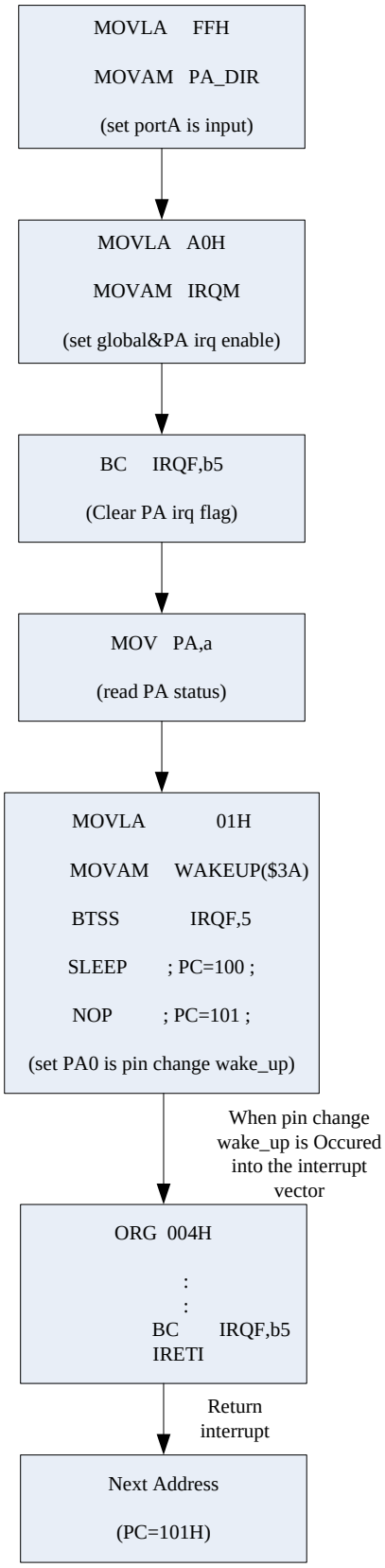
Port A (PA) provide external interrupt and wake up function. When device is not in sleep mode, the PA input single will serve as external interrupt. When external interrupt is occurred, program will jump to 004H (Interrupt vector). If device is in sleep mode, the PA input single will serve as wake up function. When wake up single input, device will let system clock work at first. Then wait for wake up timer (set by WDT_CTL register $3DH) overflow. After that, program will jump to 004H. The below flow chart describe how to set port A to work as external interrupt or wake up function.

Figure. Port A wake_up and external interrupt setting flow

Pin change (portA) interrupt :



Pin change (portA) wake up :



6.8 ADC

The BT1841 provide 12 channels and 15-bits(11bit + 4bit) resolution A/D converter. The A/D converter contains 5 registers which are AD_CTL1 (29H), AD_CTL2 (2AH), AD_CTL3 (2BH), AD_DATL (2DH), and AD_DATH(2EH).

A.AD CTL1 ($29H)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_CTL1	EN	--	MODE	--	CHSEL3	CHSEL2	CHSEL1	CHSEL0

- Bit7 (EN): ADC enable bit

  0: ADC disable.

  1: ADC enable.

<Note> When end of conversion, this bit will reset to “0” automatically.

- Bit5 (MODE): ADC mode select bit

  0: ADC channels work as A/D conversion.

  1: ADC channels work as comparator

<Note> (a) If this bit is “1”, Vin data will compare with AD_DAT. The result was stored at the AD_CTL2 Bit7. If this bit is “0”, the Vin was converted into 15-bit digital data and saved in AD_DAT register.

(b) Vin: Input voltage from ADC channel

- Bit3~0 (CHSEL3~0): ADC input channel select bits

Bit3	Bit2	Bit1	Bit0	Input channel
CHSEL3	CHSEL2	CHSEL1	CHSEL0	
0	0	0	0	Channel 0, PA0 pin
0	0	0	1	Channel 1, PA1 pin
0	0	1	0	Channel 2, PA2 pin
0	0	1	1	Channel 3, PA3 pin
0	1	0	0	Channel 4, PA4 pin
0	1	0	1	Channel 5, PA5 pin
0	1	1	0	Channel 6, PA6 pin
0	1	1	1	Channel 7, PA7 pin
1	0	0	0	Channel 8, PC7 pin
1	0	0	1	Channel 9, PD1 pin
1	0	1	0	Channel 10, PD2 pin
1	0	1	1	Channel 11, PD3 pin

B.AD_CTL2 ($2AH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_CTL2	RSUT	--	--	--	--	--	CKSEL1	CKSEL0

- Bit7 (RSUT): Compare mode result bit.

  0: Vin ＜ AD_DAT.

  1: Vin ≧ AD_DAT

- Bit1~0 (CKSEL1~0) : ADC Conversion clock source select bits

Bit1	Bit0	Conversion clock
CKSEL1	**CKSEL0**	
0	**0**	**System clock X2**
0	**1**	**System clock X8**
1	**0**	**System clock X32**
1	**1**	**System clock X128**

<Note> The conversion clocks decide the conversion rate and precision. If fast conversion clock is selected, that will drop-off the precision. If user wants to get more accurate A/D data, use slower speed is recommended.

C.AD_CTL3 ($2BH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_CTL3	**--**	**--**	**--**	**--**	**PISEL3**	**PISEL2**	**PISEL1**	**PISEL0**

- Bit3~0 (PBSEL3~0): ADC Channel input mode select bits, to set each port is analog or digital input

Bit3	Bit2	Bit1	Bit0	configurations
PISEL3	**PISEL2**	**PISEL1**	**PISEL0**	
0	**0**	**0**	**0**	**All the ports are digital input**
0	**0**	**0**	**1**	**AN0**
0	**0**	**1**	**0**	**AN1**
0	**0**	**1**	**1**	**AN2**
0	**1**	**0**	**0**	**AN3**
0	**1**	**0**	**1**	**AN4**
0	**1**	**1**	**0**	**AN5**
0	**1**	**1**	**1**	**AN6**
1	**0**	**0**	**0**	**AN7**
1	**0**	**0**	**1**	**AN8**
1	**0**	**1**	**0**	**AN9**
1	**0**	**1**	**1**	**AN10**
1	**1**	**0**	**0**	**AN11**

<Note> To minimize power consumption, all the I/O pins should be carefully managed before entering sleep mode.

D. AD_DATL (2CH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_DATL	D7	D6	D5	D4	D3	D2	D1	D0

<Note> This register has two different usage. If work in compare mode, this data will compare with input voltage from ADC channel. In ADC mode, the registers stored the ADC conversion data.

E.AD_DATH (2DH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD_DATH	--	D14	D13	D12	D11	D10	D9	D8

<Note> This register has two different usage. If work in compare mode, this data will compare with input voltage from ADC channel. In ADC mode, the registers stored the ADC conversion data.

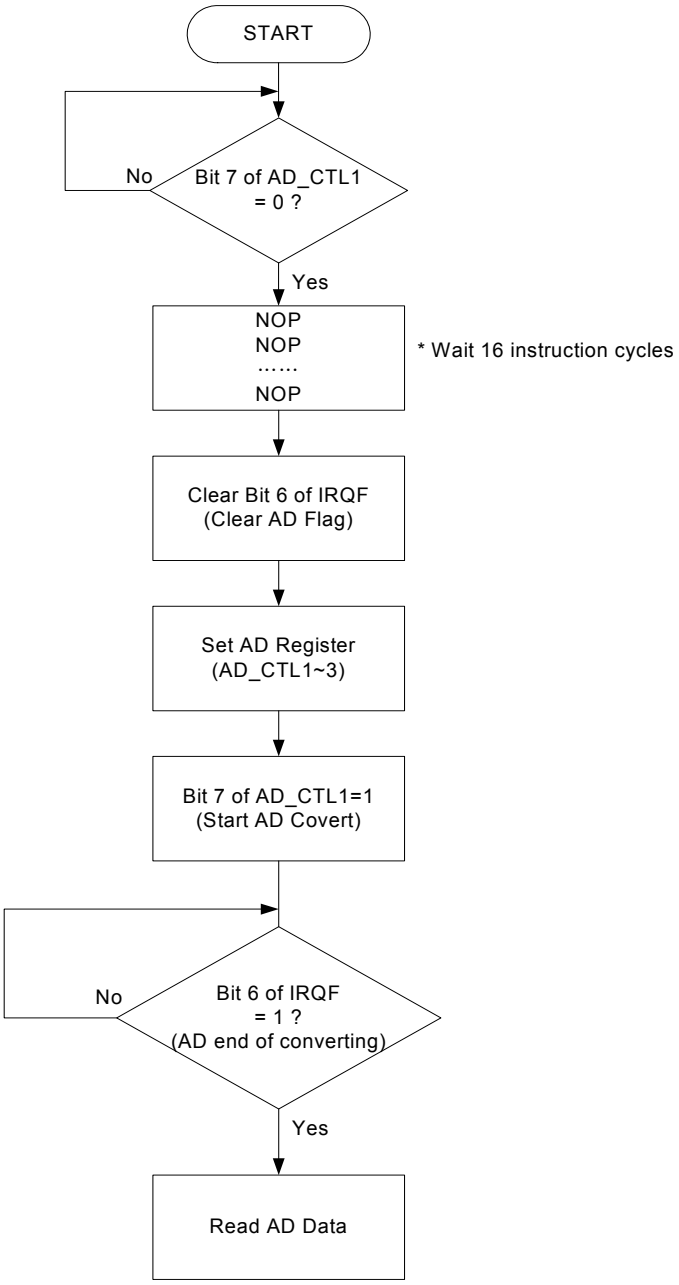


Figure. ADC setting flow

6.9 Table Look-up Function

The BT1841 provide table look-up function. The look-up tables can be placed at any location in the ROM space. The instruction of TABRDL is to read low byte of ROM table. And The TABRDH is to read high byte. The register of TAB_BNK is used to define address of high bit (MSB) of table location (3+8=11bits-address bit, 2^{11}=2Kbytes-data byte).

6.9.1 TAB_BNK ($3EH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAB_BNK	--	--	--	--	--	BANK2	BANK1	BANK0

- Bit2~0 (BANK2~0): High byte Table location select bits

Bit2	Bit1	Bit0	BANK select
BANK2	BANK1	BANK0	
0	**0**	**0**	**000 XXXX XXXX Table location**
0	**0**	**1**	**001 XXXX XXXX Table location**
0	**1**	**0**	**010 XXXX XXXX Table location**
.	**.**	**.**	**.**
1	**1**	**1**	**111 XXXX XXXX Table location**

6.9.2 Table look up Example program

The below program is an example to show how to program table looking-up function. The results of TABRDL and TABRDH will be 55H and AAH (Address is 0704H).

```
#DEFINE     TAB_BNK   3EH       ; Define address 3EH of RAM named TAB_BNK

 BUFA       EQU       43H       ; Define address 43H of RAM named BUFA

(address)   ORG       0700H     ; Program start from 0700H of ROM
 0700H      MOVLA     00H       ; Save 00H to A register
 0701H      DW        1122H     ; Store 1122H at 0701H of ROM
 0702H      DW        3344H     ; Store 3344H at 0702H of ROM
 0703H      DW        6677H     ; Store 6677H at 0703H of ROM
 0704H      DW        55AAH     ; Store 55AAH at 0704H of ROM

            MOVLA     04H       ; Save 04H to A register (low bit address)
            MOVAM     BUFA      ; Save A register's value to BUFA
            MOVLA     0FH       ; Save 0FH to A register (high bit address)
            MOVAM     TAB_BNK   ; Save A register's value to TAB_BNK
            TABRDL    BUFA      ; Looking-up the Low-byte value of TAB_BNK and BUFA
                                  pointed address, saved it to A register.

            TABRDH    BUFA      ; Looking-up the High-byte value of TAB_BNK and BUFA
                                  pointed address, saved it to A register.
```

6.10 System Control

The BT1841 provide Auto-Bank function and dual clock operation mode. Auto-Bank means when program jumping, system will automatically save the high byte of PC to prevent from carry over to cause program counter error. The dual clock mode has internal RC and external crystal clock source. User can use dual clock in the same time. For example, internal RC (4MHz) used to be system clock source, external crystal (32KHz) used to be counter clock source.

6.10.1 SYS_CTL ($3FH)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYS_CTL	CLKS	--	--	--	--	--	STPRC	STPOSC

- Bit7 (CLKS): System clock source select bit. Only active in dual clock mode (Internal RC 4MHz and Crystal) or dual RC mode (Internal RC 4MHz and external RC).

  Dual clock mode:

  0: System clock is internal RC 4MHz.

  1: System clock is OSC (if dual clock mode) or external RC(if dual RC mode).

  Single clock mode:

  Don't use.

- Bit1 (STPRC): RC (Internal RC 4MHz) oscillator control bit.

  Dual clock mode or dual RC mode:

  0: 4MHz RC oscillation on.

  1: 4MHz RC oscillation off.

  The other mode:

  Don't use.

<Note> Before setting RC oscillation off, CLKS should be switched to OSC oscillation at first.

- Bit0 (STPOSC): OSC (crystal) oscillator control bit

  Dual clock mode or dual RC mode:

  0: External OSC oscillation on (if dual clock mode) or External RC on (if dual RC mode).

  1: External OSC oscillation off (if dual clock mode) or External RC on (if dual RC mode)

  The other mode:

  Don't use.

<Note> Before setting OSC oscillation off, CLKS should be switched to RC oscillation at first.

6.11 Program Counter – PC

The M BT1841 has an 11-bits program counter (PC) that includes PCL (8-bits) and PCH (3bits). PC is used to store the routing of program. Once user changes the value of PCL, then program will jump to the indicated location. Ex1: PCH=01H, PCL=02H+10H=12H, the program will jump to PC=112H.

Ex2: PCH= 01H, PCL=F0H+30H=20H with carry 1, the program will jump to PC=220H but PCH still be 01H.

<Note> (a) When execute IRET and IRETI, PCH data would not be updated

(b) When execute LGOTO, LCALL and RET, PCH would be updated after mathematic operation

Example 1:

The below program is show how PCL and PCH working with direct mathematic operation.

```
#DEFINE     PCL     01H     ; Define address 01H of RAM named PCL
#DEFINE     PCH     02H     ; Define address 02H of RAM named PCH
#DEFINE     ADMIN   41H     ; Assist for PCL operation.

  (address)
     1C0H   MOVLA   HIGH P1 ; Save P1 (1C6H) High-byte address to A register
                            ; PC=1C0H, PCL=C0H, PCH=00H
     1C1H   MOVAM   PCH     ; Save A register to PCH (To avoid jumping error at PCL
                            operation, store the real jumping high-byte address to PCH
                            at first.)
                            ; PC=1C1H, PCL =C1H, PCH=01H.
     1C2H   MOVLA   4BH     ; Save 4BH to A register (Address of ADDAM PCL,M is
                            1C5H, prepare jump to 210H, PCL have to add 210H-1C5H
                            =4BH)
                            ; PC=1C2H, PCL =C2H, PCH=01H.
     1C3H   MOVAM   ADMIN   ; Ready for PCL operation.
                            ; PC=1C3H, PCL =C3H, PCH=01H.
     1C4H   DEC     ADMIN, a ; ADMIN –1 (The real jumping happen at 1C6H, not 1C5H.
                            So 1C6H+(4BH-1H) =210H)
                            ; PC=1C4H, PCL =C4H, PCH=01H.
     1C5H   ADD     PCL,M   ; PCL add with A register, result store at PCL
                            ; PC=1C5H, PCL =C5H, PCH=01H
   P1: 1C6H   NOP           ; Jump to 0210H.
                            ; PC=1C6H, PCL=C6+4AH=10H with carry in 1,the carry
                            will count with PCH, PCH=01H, the purpose PC high
                            byte address will be  PCH + PCL's carry=02H. The
                            program will jump to PC=210H
     210H   MOVLA   00H     ; Purpose function part.
                            ; PC=210H, PCL =10H, PCH=01H
```

Example 2:

The below program is show how PCL and PCH working with direct mathematic operation.

```
(address)
   1C0H   MOVLA    03H        ; Save 03H to A register
                              ; PC=1C0H, PCL=C0H, PCH=00H
   1C1H   MOVAM    PCH        ; Save A register to PCH
                              ; PC=1C1H, PCL =C1H, PCH=03H.
   1C2H   MOVLA    4BH        ; Save 4BH to A register
                              ; PC=1C2H, PCL =C2H, PCH=03H.
   1C3H   MOVAM    ADMIN      ; Ready for PCL operation.
                              ; PC=1C3H, PCL =C3H, PCH=01H.
   1C4H   DEC      ADMIN, a   ; ADMIN –1 (The real jumping happen at 1C6H, not 1C5H.
                              So 1C6H+(4BH-1H) =210H)
                              ; PC=1C4H, PCL =C4H, PCH=03H.
   1C5H   ADD      PCL,M      ; PCL add with A register, result store at PCL
                              ; PC=1C5H, PCL =C5H, PCH=03H
   1C6H   NOP                 ; Jump to 410H.
                              ; PC=1C6H, PCL=C6+4AH=10H with carry in 1,the carry
                              will count with PCH, PCH=03H, the purpose PC high
                              byte address will be  PCH + PCL's carry=04H. The
                              program will jump to PC=410H
   410H   MOVLA    00H        ; Purpose function part.
                              ; PC=410H, PCL =10H, PCH=03H
```

Example3

The below program is show how PCL and PCH working through A register

```
(address)
   018H   MOVLA    02H        ; Save 02H to A register
   019H   MOVAM    PCH        ; Save A register to PCH(The purpose address is 200H, so
                              store "02H" to PCH)
   01AH   MOVLA    00H        ; Save 00H to A register
   01CH   MOVAM    PCL        ; Save A register to PCL(The purpose address is 200H, so
                              store "00H" to PCL)
   01DH   NOP                 ; Jump to 200H.

   200H   MOVLA    00H        ; Purpose function part.
```

6.12 STATUS Register

The STATUS register is an 8-bit register that contains the zero flag (Z), carry flag (C), Nibble carry flag (DC), power down flag ($\overline{PD}$), and watchdog timer overflow flag ($\overline{TO}$). It records the status information.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	--	--	--	$\overline{TO}$	$\overline{PD}$	Z	DC	C

- Bit4 ($\overline{TO}$): Timer overflow flag bit
- Bit3 ($\overline{PD}$):Power down flag bit

$\overline{TO}$	$\overline{PD}$	Description
0	0	WDT timer overflow from sleep mode
0	1	WDT timer overflow from normal mode
1	0	Input a ‘low” at RESETB from sleep mode
1	1	Power on reset
Unchanged	Unchanged	Input a “low” at RESETB from normal mode

- Bit2 (Z): zero flag bit

  0: The result of a logic operation is not zero

  1: The result of a logic operation is zero

- Bit1 (DC): Nibble Carry and Nibble $\overline{Borrow}$ flag bit

  ADD instruction:

  0: No nibble carry occurred

  1: Nibble carry occurred

  SUB instruction

  0: Nibble borrow occurred

  1: No nibble borrow occurred

- Bit0 (C): Carry and $\overline{Borrow}$ flag bit

  ADD instruction:

  0: No carry occurred

  1: Carry occurred from the MSB

  SUB instruction

  0: Borrow occurred from the MSB

  1: No borrow occurred

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V Storage Temperature ……. –40℃ to 125℃

Input Voltage …… Vss-0.3V to VDD+0.3V Operating Temperature… – 40℃ to 85℃

<Note>: These are stress ratings only. Stresses exceeding the range specified under ”Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

8.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---	f_{sys} =4MHZ	2.0		5.5	V
			f_{sys} =8MHZ	2.5		5.5	
			f_{sys} =12MHZ	3.3		5.5	
I_{DD1}	Operating Current (Crystal OSC)	3.3V	No Load , f_{sys} =32KHZ ADC disable		10		uA
		5V			26		
I_{DD2}	Operating Current (Crystal OSC)	3.3V 5V	No Load , f_{sys} =4MHZ ADC disable		0.8 1.7		mA
I_{DD3}	Operating Current (RC OSC)	3.3V	No Load , f_{sys} =4MHZ ADC disable		0.8		mA
		5V			1.4		
I_{DD4}	Operating Current (Crystal OSC)	5V	No Load , f_{sys} =8MHZ ADC disable		3		mA
I_{DD5}	Operating Current (Crystal OSC)	5V	No Load , f_{sys} =12MHZ ADC disable		4.2		mA
V_{IH}	Input High Voltage	5V	I/O Port	2		VDD	V
V_{IL}	Input Low Voltage	5V	I/O Port			0.8	V
I_{STB}	Standby Current	5V	WDT disable			1	μA
			WDT enable			6	
		3V	WDT disable			1	
			WDT enable			2	

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS			1	μA
I_{OH}	I/O Port Driving Current	5.5V	Voh=5V			9.9	mA
			Voh=4.5V			17.6	
			Voh=4V			24.8	
I_{OL}	I/O Port Sink Current	5.5V	Vol=0.5V			24.5	mA
			Vol=0.75V			35.3	
			Vol=1V			43.8	
R_{PH}	Pull-high Resistance	3V		80	100	120	KΩ
		5V		30	50	70	KΩ
V_{AD}	A/D input Voltage	--		0		VDD	V
R_{AD}	Resolution					15	Bits
DNL	A/D Differential Non-Linear	--				4	LSB
INL	A/D Integral Non- Linear	--				6	LSB
I_{ADc}	A/D Operating Current	3.3V			200		uA
		5V			700		
V_{OSV}	Comparator Input Offset Voltage	--		-30	--	30	mV
V_{CI}	Comparator Input Voltage Range	--		0.2	--	VDD-0.7	V

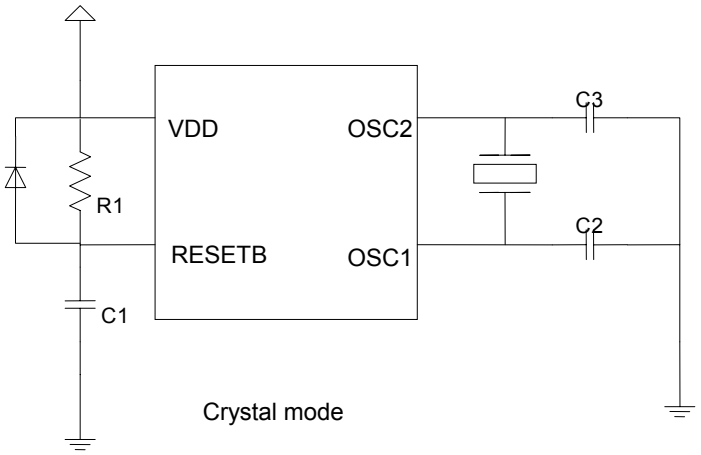
8.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		Conditions	VDD				
f_{sys1}	System Clock	LS Crystal mode	5V	32		200	Khz
			3V	32		200	
f_{sys2}	System Clock	NS Crystal mode	5V	0.2		10	Mhz
			3V	0.2		10	
f_{sys3}	System Clock	HS Crystal mode	5V	10		20	Mhz
f_{sys4}	System Clock	RC mode	5V	3.4	4	4.6	Mhz
			2.2V	3.4	4	4.6	
T_{wdt}	Watchdog Timer		5V		20		mS
			3V				
T_{rht}	Reset Hold Time		5V		20		mS
			3V				
T_{AD}	A/D clock period			3			us
T_{ADC}	A/D Conversion Time				34		t_{AD}
T_{ADCS}	A/D Sampling Time				8		t_{AD}
F T_{AD}	A/D clock period(Fast mode)	System-clk=4MHZ, Clksel=01(4MHZ/8)		2			us
F T_{ADC}	A/D Conversion Time (Fast mode)				50		us
F R_{AD}	Resolution (Fast mode)					8	MSB
T_{COMP}	Comparator Response Time					3	us

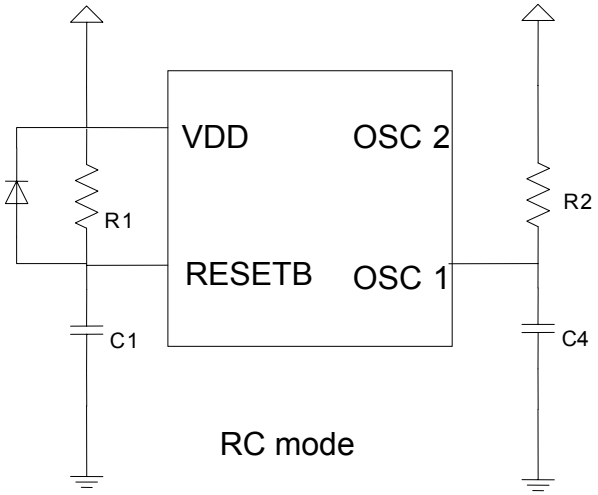
8.4 External RC Table

R value(R2)	C value (C4)	RC Frequency	R connect to (VDD, OSC1)
4.9M	0.1u (need)	32KHZ	The capacitor is need for stabile frequency
250K	0.1u (suggest)	455KHZ	
116K	0.1u (suggest)	1MHZ	
60K	0.1u (suggest)	2MHZ	
32K	0.1u (suggest)	4MHZ	
18K	0.1u (suggest)	8MHZ	
14K	0.1u (suggest)	10MHZ	

8.5 Oscillator circuit in different mode



Crystal mode



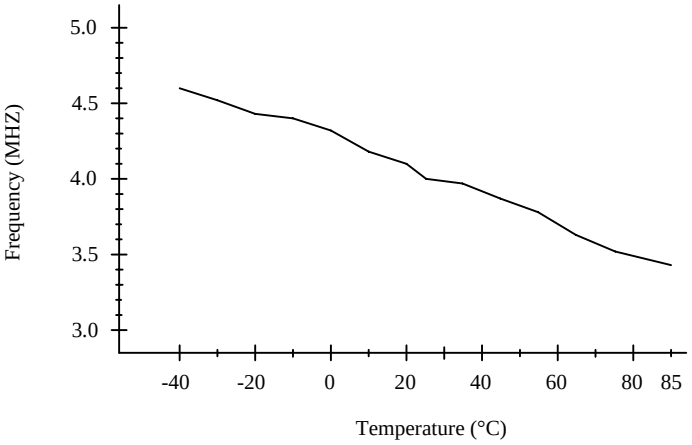
RC mode

Crystal mode	Crystal	C2	C3
LP mode	32 Khz	20~100P	20~100P
	455 Khz	100P	100P
NT mode	455 Khz	100P	100P
	1 Mhz	20~100P	20~100P
	2 Mhz	20~100P	20~100P
	4 Mhz	20~100P	20~100P
	8 Mhz	20~50P	20~50P
	10 Mhz	20~50P	20~50P
HS mode	12 Mhz	20~50P	20~50P
	16 Mhz	20~50P	20~50P
	20 Mhz	20~50P	20~50P

8.6

Internal RC Electrical Characteristics
(Ta= -40°C ~ 85°C , VDD=2.2V ~ 5.5V , VSS=0V)

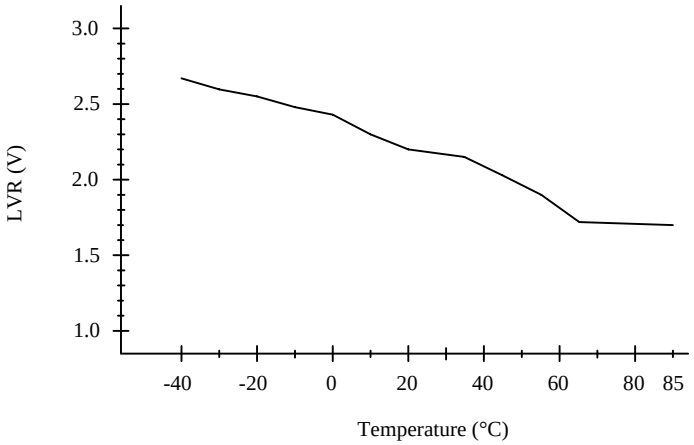
Voltage	2.2V ~ 5.5V		
Temperature	-40°C	25°C	85°C
Internal RC	4.6MHZ	4MHZ	3.4MHZ

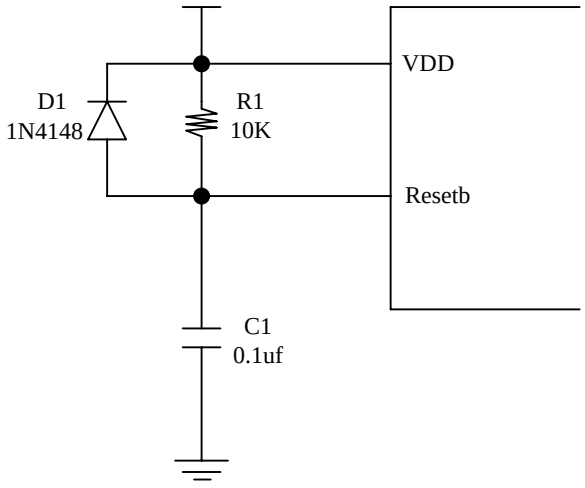


8.7

LVR Electrical Characteristics
(Ta= -40°C ~ 85°C)

LVR	2V		
Temperature	-40°C	25°C	85°C
LVR	2.67V	2.17V	1.7V

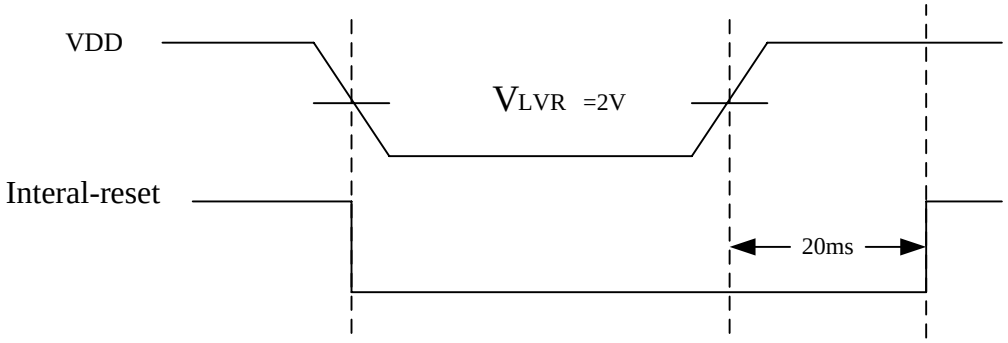




Reset Circuit

Timming :

1. LVR on



2. LVR off