UART IP CORE

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UART IP core – Specifications

- 8-bit
- Programmable baud rates from 600-115200
- Start, Stop bits and No parity included
- Clock input - 100 MHz
- Maximum permissible frequency mismatch for data reception = +/- 4.0%
- Maximum error in baud rate generation = +/- 0.005%
- Tested in Artix-7 FPGA for 100 MHz clock input

UART IP core - Interface signals

- Load – Pulled low, to start transmission
- Reset – Active low signal to reset the module
- Enable – Active low chip enable signal
- Clock in – Input clock
- Baud rate – To set baud rate
- Tx Data in – Parallel 8 bit data input from processor
- Tx Data out – Serial data output
- Rx Data in – Serial data input
- Rx Data out – Parallel data output to processor
- Tx intr – Transmit interrupt to processor
- Rx intr – Receive interrupt to processor
- ERROR – To indicate error in data reception

Setting baud rate

Baud rate vector input	Baud rate
0000	600
0001	1200
0010	2400
0011	4800
0100	9600
0101	19200
0110	38400
0111	57600
1000	115200

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