VGA Controller IP Core v1.0

Description

VGA Controller IP Core v1.0 is a fully configurable soft IP used in video timing generation applications. The IP can be used to generate VGA timing signals as required by the resolution selected by the user. The IP can be easily interfaced with DACs to drive VGA displays.

Features

- Configurable X and Y display resolution, front and back porches.
- Configurable X and Y sync pulses and polarities.
- The core can be clocked with the pixel clock or the system clock itself. Pixel frequency can be externally controlled using clock enable.
- Fully synthesisable and FPGA proven design.

RTL

All source files of the IP are in System Verilog.