## Xilinx XC6SLX9 Mini Board

User's Guide



## **1. Introduction**

XC6SLX9 Mini Board is an easy-to-use FPGA platform based on Xilinx Spartan 6 series FPGA. It was initially designed for low cost with a everyone affordable price. Up to 72 I/O breakout makes it suitable in high pin count applications. You can connect the I/Os to your peripheral modules with several flying wires to quickly build a prototype project. Also, one USB to UART bridge is integrated on board, only a USB cable is needed for power supply and data communication. Because of its compact size and abundant IOs, it can be easily embedded in your design as a core. This guide describes how to use Xilinx tools and XC6SLX9 Mini Board to learn FPGA as a beginner. If you are familiar with Xilinx design tools and the process of FPGA design, some sections could be ignored.

#### The XC6SLX9 Mini Board includes:

- Xilinx Spartan 6 FPGA XC6SLX9-2TQG144C(<u>Spartan-6 FPGA Family Overview</u>)
- 64-Mbit SPI Flash memory (W25Q64BV)
- USB to UART ( FT232RL ) with TXD, RXD activity LED Indicator
- Two groups of 2x20 expansion header (72 I/Os, +3.3V, +5V, GND)
- JTAG programming header, directly connected to Xilinx Platform Cable USB
- Two pushbuttons
- One reset pushbutton for reloading configuration file from external flash into FPGA
- Eight LEDs for I/O status indication
- 50 MHz clock oscillator
- USB or external power supply ( can be powered with a 9V battery )

#### Board Size: 75(mm) x 49(mm)



#### XC6SLX9 Mini Board Layout ( Top Side )

## 2. Get the tools ready

First, we must get the necessary software and hardware tools ready before starting a FPGA project. Three tools must be prepared:

- ISE WebPACK Design Software We use HDL( Hardware Description Language ) code like Verilog or VHDL to describe a digital circuit, code must be compiled and ultimately implemented into a circuit layout that can be programmed to FPGA device. ISE WebPACK Design Software is an fully integrated tool for this purpose provided by Xilinx.
- XC6SLX9 Mini Board and one mini USB cable This board includes a target FPGA device and some other necessary circuitry and peripherals to support the running of the device.
- 3) Xilinx Platform Cable USB or a parallel download cable This is a programming tool to download an configuration file generated by ISE WebPACK to the internal SRAM of the target FPGA device or an external non-volatile memory.

### 2.1 Download and Install ISE WebPACK Design Software

Xilinx provides a free IDE software named ISE WebPACK for beginners. Although it has limited functions compare to other charged editions, but that's enough for most beginners. It's a complete solution for FPGA design offering HDL synthesis and simulation, implementation, device fitting, and JTAG programming. Please visit <u>ISE</u> WebPACK Design Software webpage for details and <u>download</u> it to you PC. Different versions are provided, but they have similar UI and basic functions. Of course the latest version will occupy more hardware disk space. So which version you choose depends on your PC. We use ISE WebPACK 14.1 for demonstration in this guide.

Note: If you have installed ISE WebPACK Software on your PC, you can ignore this section.

All the operations in the following sections are done on Windows 8.1 x64 operating system.

### 2.2 Install the ISE WebPACK Design Software

1) Unzip the download file and go to the setup directory, double-click **xsetup.exe** to start the installation process.

i autorun.inf	4/24/2012 2:35 PM	Setup Information	1 KB
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xsetup	4/24/2012 2:35 PM	File	1 KB
🕻 xsetup.exe	4/24/2012 2:36 PM	Application	748 KB

2) A welcome window appears, click **Next** to next window.



3) Enable the checkbox to accept terms and conditions, click **Next** to next window.



 Another license agreement window appears, enable the check box, and click Next to next window.



 Differnent editions are contained in this ISE Design Suite. We select ISE WebPACK. Click Next to next window.

<u>1</u>	ISE Design Suite 14.1 Installer – 🗖 🗙
	Select Edition to Install
	È- Edition List
	● ISE WebPACK
	-C ISE Design Suite: Logic Edition
DESIGN SUITE	-C ISE Design Suite: Embedded Edition
	-C ISE Design Suite: DSP Edition
	C ISE Design Suite: System Edition
	C Software Development Kit: Standalone Installation
	C Lab Tools: Standalone Installation
ISE Design Suite 14.1 Installer	
Welcome	Dick Control Description 14014 MD
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-> Select Edition to Install	
Select Installation Options	Description of ISE WebPACK
Select Destination Directory	ISE WebPACK contains the most important tools you need for designing CPLDs and small to medium-sized FPGAs. Includes: ISE Design Tools (w/reduced device support), PlanAhead, and Connectivity and DSP IP. ChipScope Pro and The Embedded Development Kit will also be installed with WebPACK but are licensed separately (not included in a WebPACK license file).
Copyright (c) 1995-2012 Xilinx, Inc. All right reserved. XILINX, the Xilinx logo and other designate brands included herein are trademarks of Xilin Inc. All other trademarks are the property of their respective owners.	s d c f
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6) Select the options as shown below. Click **Next** to next window.

<u>11</u>	ISE Design Suite 14.1 Installer 🛛 🗕 🗖 🗙
	Select Installation Options Select the desired installation options below. Selection of these options may result in additional programs being run at the conclusion of the installation process.
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	Acquire or Manage a License Key     Sourcery CodeBench for Xilinx Cortex-A9 GNU/Linux     Sourcery CodeBench for Xilinx Cortex-A9 EABI     Install WinPCap for Ethernet Hardware Co-simulation
ISE Design Suite 14.1 Installer	✓ Install Cable Drivers
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Select Destination Directory	Select/Deselect All
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	Cable drivers are required to ensure proper operation of the parallel and USB cables when configuring Xilinx devices. Please disconnect any Xilinx cables from your machine prior to driver installation.
Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.	
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7) Select destination directory. You can change to other directory if you don't have enough space in C disk. Click **Next** to next window.

-	ISE Design Suite 14.1 Installer		-		x
ESIGN SUITE	Select Destination Directory Select the directory where you want the software installed. C:\Xillinx Disk Space Required : 14314 MB Disk Space Available : 18443 MB	Browse			
ISE Design Suite 14.1 Installer Welcome Accept License Agreements Select Edition to Install Select Installation Options -> Select Destination Directory Installation	Select a Program Folder This name will appear in the Start Menu > Programs list. Xilinx Design Tools Import tool preferences from previous version and change project file association to ISE WebPACK 14.1				•
Copyright (c) 1995-2012 Xilinx, Inc. All right reserved, XILINX, the Xilinx logo and other designates brands included herein are trademarks of Xilinx Inc. All other trademarks are the property o their respective owners.		K Back N	ext >	Cance	5

8) A summary window lists the tools and components that will be installed, click **Install** to start the installation.



9) It may take several minutes to complete the installation, please wait patiently.



10) A message box may pop up to inform you to disconnect all Xilinx Platform cables. Remove the cables and Click **OK**.

\$ <u>2</u>	ISE Design Suite 14.1 Installer [ 91% ] – 🗆 🗙
* XILINX. ISE DESIGN SUITE	ISE: Install Cable Drivers 91%
ISE Design Suite 14.1 Installer	Vivado™ Cable Driver Installer
Welcome Accept License Agreements Select Edition to Install Select Installation Options Select Destination Directory -> Installation	Please disconnect all Xilinx Platform Cable USB or Evaluation Platform JTAG cables from this system before continuing.
	Perform block-based design using pre-routed IP for true team design
Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo and other designated brands included herein are trademarks of Xilinx Inc. All other trademarks are the property of their respective owners.	www.xiiinx.com/products/intellectual-property
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#### 11) Click **Finish** to complete the the installation.

2	ISE Design Suite 14.1 Installer [ 100% ] – 🗖 🗙
<b>SILINX.</b> <b>ISE</b> DESIGN SUITE	Install Completed Congratulations! You have successfully installed Xilinx ISE WebPACK. The environment variables are written to the .settings[32]64] bat file for each application and an encompassing settings[32]64], bat at "C.Xilinx114.1\SE_DS". In order to set the variables in your environment, you must source the settings[32]64], bat file from "C.Xilinx114.1\SE_DS". The shortcuts created by the ISE Design Suite Installer source the appropriate settings script prior to launching each tool. Command line and script users should source the settings script prior to launching the tools.
ISE Design Suite 14.1 Installer Welcome Accept License Agreements Select Edition to Install Select Installation Options Select Destination Directory -> Installation	
Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo and other designated brands included hereina retrademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.	
	Finish

- 12) To Get a free license from Xilinx, you must register a user account on Xilinx Website and apply for a free license for ISE WebPACK. The details are ommited here, just follow the instructions on the website, you will get the license file easily.
- 13) After receiving a license from Xilinx, copy the license file to the destination directory where the software is installed. Enter Manage Xilinx Licenses tab, click Copy License..., and then locate the license file with .lic suffix.

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14) Congratulations! You have successfully installed and activated the software.



### 2.3 Setup the XC6SLX9 Mini Board

A USB connection is provided on XC6SLX9 Mini Board. It is intended for data communication and powering the board. FT232R is used as a USB to UART bridge. It is a very popular IC widely used in various USB converter cables. As usual, a device driver software must be installed before the operating system could successfully recognize and operate the device.

#### Note:

- 1) If your PC has the driver software installed before, the on-board FT232R will be enumerated as a common serial port when you connect the board to PC.
- 2) For the latest operating system like Windows 8, when a USB device detected, it will automatically find and install the driver for the device if windows update is enabled and internet connection is available.

The following instructions describe how to install the driver software for FT232R:

#### 1) Power the board

Plug the XC6SLX9 mini board to your PC via a USB mini cable. When powered, the windows system will detect the insertion of a USB device and try to load a driver for this device. If windows fail to find the driver, it will list the device in the Device manager with a yellow exclamation mark, indicating the driver for this device is not found.

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Print queues		
Processors		
Sensors		
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G= Storage controllers		
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Universal Serial Bus controllers		
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#### 2) Install driver software automatically(Internet connection must be available)

- Right click on the FT232R USB UART, and select **Update Driver Software...**
- Select Search automatically for updated driver software
- Windows will automatically find and install the driver software, this will take a few seconds.

#### 3) Install driver software manually

- <u>Download</u> the driver software from FTDI website according to the edition of your operating system.
- Now, for Windows system, an executable version of this driver is available, unzip and run the executable file, driver will be installed automatically.

#### 4) Verify the result

If the driver software is properly installed, the FT232R will function as a virtual serial port. And it will appear in the Device Manager list.



Note: You must get a serial port monitor software like PuTTY to hunt the serial port activities.

### 2.4 Setup Xilinx Platform Cable

A download cable is needed to program the configuration file to the target FPGA device. Xilinx provides USB download cable and parallel download cable, but USB cable is more popular because parallel port is eliminated in most new generation desktop or laptop PCs. We use Xilinx Platform Cable USB in all the demos and examples. A USB driver software is needed for this cable. It's integrated in the ISE WebPACK Design Software and has been installed in previous installation process. If the driver doesn't work or crashed, please read the application guide USB Cable Installation Guide, and reinstall it. If driver software is properly installed, the cable named Xilinx USB Cable will appear in the Device Manager list.





## **3. Create your first FPGA Project**

This section will guide you through the process of creating a simple FPGA project using Verilog HDL. We build an 8-bit barrel shifter that rotates one bit to the right in the interval of 1/4 second. The state of the shifter will be displayed on the eight LEDs. And finally, the object file will be downloaded to the target device on XC6SLX9 Mini Board and got verified.

*Note:* Some procedures like simulation, timing analysis, and creating constraints in FPGA design are omitted in this section.

1) Double-click **ISE Project Navigator** icon to start the IDE.



2) Select File -> New Project... The New Project Wizard appears.



3) Type Barrel\_Shifter in the Project Name field. Browse to a location (directory path) for the new project. A Barrel\_Shifter subdirectory will be created automatically. Select HDL in the Top-Level Source Type list. Click Next to move to the device property window.

>	New Project Wizard	X
Ereate New Project Specify project lo	t cation and type.	
Enter a name, locati	ions, and comment for the project	
Name:	Barrel_Shifter	
Location:	C:\Users\Adam\Desktop\XC6SLX9 Mini Board Examples\Barrel_Shifter	
Working Directory:	C:\Users\Adam\Desktop\XC6SLX9 Mini Board Examples\Barrel_Shifter	
Description:	This example shows a simple 8-bit barrel shifter that rotates one bit to the right in the interval of 1/4 second. The state of the shift register is displayed on 8 LEDs.	
Select the type of to	op-level source for the project	_
Top-level source typ	pe:	
HDL		~
More Info	Next >	Cancel

4) Select a value for Device, Package, Speed and other properties as shown below.

Property Name     Value       Evaluation Development Board     None Specified       Product Category     All       Family     Spartan6       Device     XC65LX9       Package     TQG144       Speed     -2       Top-Level Source Type     HDL       Synthesis Tool     XST (VHDL/Verilog)       Simulator     ISim (VHDL/verilog)       Preferred Language     Verilog	perty Name Value v	elect the device and design flow for the p	project	
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5) A summary window appers.Click finish to comlete the project wizard.

New Project Wizard
Project Summary Project Navigator will create a new project with the following specifications.
Project: Project Name: Barrel_Shifter Project Path: C:\Users\Adam\Desktop\XC6SLX9 Mini Board Examples\Barrel Working Directory: C:\Users\Adam\Desktop\XC6SLX9 Mini Board Examples\B Description: This example shows a simple 8-bit barrel shifter that rot Top Level Source Type: HDL
Device: Device Family: Spartan6 Device: xc6slx9 Package: tqg14 Speed: -2
Top-Level Source Type: HDL Synthesis Tool: XST (VHDL/Verilog) Simulator: ISim (VHDL/Verilog) Preferred Language: Verilog Property Specification in Project File: Store all values Manual Compile Order: false VHDL Source Analysis Standard: VHDL-93
Message Filtering: disabled
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More Info Cancel

6) Click **Project -> New Sources...** to create an HDL source.

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7) Select Verilog Module, enter the file name Barrel\_Shifter. Leave the file location to the default. Verify that the Add to project checkbox is selected. Click Next to next window.

> New Sour	ce Wizard	×
Select Source Type Select source type, file name and its location.		
<ul> <li>IP (CORE Generator &amp; Architecture Wizard)</li> <li>Schematic</li> <li>User Document</li> <li>Verilog Module</li> <li>VHDL Module</li> <li>VHDL Module</li> <li>VHDL Library</li> <li>VHDL Package</li> <li>VHDL Test Bench</li> <li>Embedded Processor</li> </ul>	File name: Barrel_Shifter Location: C:\Users\Adam\Desktop\XC6SLX9 Mini Board Example	
More Info	Next > Cancel	

8) Declare the input and output ports for the module as shown below, and then click Next to next window.

•	٩	New Source Wizard	I							
Cefine Module Specify ports for module.										
Module name	Barrel_Shifter									
	Port Name	Directio	n	Bus	MSB	LSB	^			
CLK_50M		input	¥							
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LED		output	~	•	7	0				
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		input	~				~			
More Info	]		< Ba	ack	Next >	Canc	el			

**9)** A summary window displays the information you entered in previous steps. Click **Finish** to complete the wizard if no errors found.

>			New Source	e Wizard			×		
Summary Project Navigator will create a new skeleton source with the following specifications.									
Add to Project: Yes Source Directory: C:\Users\Adam\Desktop\Examples\Barrel_Shifter Source Type: Verlig Module Source Name: Barrel_Shifter.v									
Module name: Port Definition	Barrel_Shifter								
	CLK_50M Reset LED	Pin Pin Bus:	7:0	input input output					
More Info	]			< Ba	ack	Finish	Cancel		

**10)** The module head and some comments about this module have been added to the source code file automatically.

>	ISE Project Navigator (P.15xf) - C.\Users\Adam\Desktop\XC65LX9 Mini Board Examples\Barrel_Shifter\Barrel_Shifter\ser-[Barrel_Shifter\ve_]	- 8 ×
File Edit View Project Source Process	s Tools Window Layout Help	_ # ×
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> Start 🔍 Design 🐚 Files 🐚 Libraries	Barrel Shiftesv <sup>a</sup>	,
Console		+- D # ×
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		Ln 11 Col 19 Verilog

11) Copy the HDL code shown below to the Barrel\_Shifter source file and save the file.

Note: If you are new to Verilog HDL and can't understand the meaning of the code, please don't worry about that. You will get familiar with the coding rules after reading a Verilog HDL book. We mainly focus on learning the tools of Xilinx FPGA, not the details of Verilog HDL in this guide.

```
module Barrel_Shifter( input CLK_50M, input Reset, output [7:0] LED );
reg [23:0] counter;
          shift_reg = 8'b0000_0001;
reg [7:0]
always@(posedge CLK_50M)
begin
  if(Reset)
  begin
      counter \leq 0;
  end
  else
      counter <= counter + 1'b1;
end
always @(posedge CLK_50M)
begin
  if(Reset)
      shift_reg <= 8'b0000_0001;
  else
  begin
  if( counter == 24'b1011_1110_1011_1100_0010_0000 )
      shift_reg <= { shift_reg[6:0],shift_reg[7] };</pre>
  end
end
assign LED[7:0] = shift_reg[7:0];
endmodule
```

**12)** Double-click **Implement Design** in the process window. The project will be parsed and synthesized successfully.

If the first war hour hour hour hour hour hour hour hou	>			ISE Project Navigato	r (P.15xf) - C:\Users\Adam\Desktop\XC6SLX	9 Mini Board Examples\Barrel_Shifter\Barrel	_Shifter.xise - [Barrel_Shifter.v*]	- 8 <mark>- X</mark>
<pre></pre>	📄 File Edit	it View Project Source Proce	as Too	ls Window Layout Help				_ # ×
Der	🗋 🏓 🖬	∰ &  X ⊡ ⊡ X  ∞ (	н 1	///////////////////////////////////////	N? 🕨 🗵 📌 💡			
<pre>     branching Desgin Humany (Net Contains + 1/Bi)     desgin Humany (Net Contain</pre>	Design Ven:  Ven:	<ul> <li>Image: Some state of the state</li></ul>		6 // Creat Ext: 12/15/20 20/24 7 // Design Band 8 // Design Band 8 // Bregiot Rese: 10 // Bregiot Rese: 11 // Bregiot Rese: 12 // Description: 13 // Description: 14 // Description: 15 // Pervision 15 // Additional Comments: 16 // Additional Comments: 17 // Additional Comments: 18 // Additional Comments: 19 // Additional Comments: 19 // Additional Comments: 10 // Additional Comments: 11 // Comments: 12 // Comments: 13 // Comments: 14 // Comments: 15 // Comments: 15 // Comments: 16 // Comments: 17 // Comments: 17 // Comments: 18 // Comments: 19 // Comments: 19 // Comments: 19 // Comments: 19 // Comments: 10 // C	2014 			~
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Grame I SITO-OBIC-Competition 1981 - Analyzing Verslog file %://Greet/Adam/Desktop/DEGLES Mini Board Examples/Barrel_Bhifter/Barrel_Bhifter/V into library work ISITO-OBIC-Competition - Paralog design hierarchy completed successfully. Detred : "Auroching ISE Test Editor to edit Barrel_Shifter.v". Examining Design Humary/Report Viewer	> Start	📲 Design 🚺 Files 🌓 Libraries		Barrel Shifter.v*	2 2	Design Summary	×	
LUBYOURDCompler:144 - Analyzing Verlig file "C/Verers/And/Destop/CEGINS Hinl Board Examples/Barrel_Bhifter.V* into likeary work JEDForbogeneties - Farang design Harardy soughested as soughestly. Bearred : "Ausonaing INT Test Editor to edit Barrel_Bhifter.V*. Exampling Dasign Hamary/Maport Viewer	Console							** • • • • • •
📗 Console 🙆 Errors 🛕 Wannings 🙀 Find in Films Raturda	<ul> <li>UNFO:HE</li> <li>UNFO:Pr</li> <li>Started</li> <li>Launchi</li> <li>Console</li> </ul>	DLCompiler:1845 - Analyzi rojectKgmt - Parsing desi d : "Launching ISE Text E ing Design Summary/Report	ng Ver pn hid ditor View Findin Fi	rilog file "C://Secr/Adm/Debtop/KC651X Tracfoly complexed successfully. to edit Barrel_Shifter.v". Nr	Mini Board Examples/Barrel_Shifter/	/Barrel_Shifter.v" into library work		, ,

Note: Since the source code is verified, you don't need to correct any syntax errors or typos. In most cases, error is unavoidable for beginners, you should learn to analyze the error or warning tips printed in the Errors and Warnings window.

13) Click Tools -> PlanAhead -> I/O Pin Planning(PlanAhead)-Post-Synthesis... to assign pin locations. Then click Yes to automatically create a new constraint file add it to project.





14) Assign pin locations as shown below and then save the constraint.

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L/D Ports													- 0 8 ×
Name Dire	ection Neg Diff Pair	Site	Fixed Ba	nk I/O Std	Vcco Vre	of Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM	OUT_TERM		
All ports (10)								and a state			1.01.0		
	put	0170		0 LVCM0533*	3.3		12 SLOW	NONE	FP_VI1_50		NONE		
LED[1] Out	put	P137	V	0 LVCM0533*	3.3		12 SLOW	NONE	FP VTT 50		NONE		
	put	P134		0 LVCMOS33*	3.3		12 SLOW	NONE	FP_VTT_50		NONE		
- G LED[3] Out	put	P133	~	0 LVCMOS33*	3.3	1	12 SLOW	NONE	FP_VTT_S0		NONE		
	put	P120	¥	0 LVCMOS33*	3.3		12 SLOW	NONE	FP_VTT_S0		NONE		
- 4 LED(5) Out	put	P118	1	0 LVCMOS33*	3.3		12 SLOW	NONE	FP VTT 50		NONE		
	put	P117	1	0 LVCMO533*	3.3		12 SLOW	NONE	FP_VTT_S0		NONE		
B Scalar ports (2)			_										
- CLK_SOM Inp	t.	P50	¥	2 LVCM0533*			12 SLOW	NONE	NONE	NONE			
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- ro console ( paraolay	Cris I/o Ports												
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- **15)** Reimplement the design.
- **16)** In the Process window, double-click the **Configure Target Device** process. The system will automatically generate an configuration file for programming, and then iMPACT software will be launched.

>	ISE Project Navigator (P.15xf) - C_Users\Adam\Desktop\XC65LX9 Mini Board Examples\Barrel_Shifter\Barrel_Shifterxise - (Barrel_Shifterxi	- 8 ×							
File Edit View Project Source Process	Tools Window Layout Help	_ # ×							
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🍃 Start 🔍 Design 🜔 Files 🌔 Libraries 👔	Berrel, Shifter. v 🖸 🔀 Design Summary (Implemented)								
Console		+□ # ×							
Analysis completed The Mar 24 09:03:47 2019 A									
LIGGERS CLICLUSE POSC-FIRGE & ROU	Process "venerate Post-Prace & Houte Static liming" completed successfully								
¢	1	>							
📱 Console 🤩 Errors 🧘 Warnings 🕷 Find	in Files Assults	Ln 40 Col 4 Verilog							

17) In the ISE iMPACT window, double-click Boundary Scan.

Note: To successfully find a device in the JTAG chain, Xilinx Platform cable USB must be connected to the XC6SLX9 Mini Board, and both should be powered.

8	ISE iMPACT (P.15xf)	- 🗆 🗡
File Edit View Operations Output Debug Wind	low Help	
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MPACT Flows ↔ □ & ×		
Boundary Scan		
SystemACE     SystemACE     Create PROM File (PROM File Format		
😥 📑 WebTalk Data		
MPACT Processes ↔		
Console		+□₽×
		^
K		×
<		>

**18)** Click the **Initialize Chain** command, iMPACT will automatically search devices available in the JTAG chain and display the result in the **Boundary Scan** window.

	ISE iMPACT (P 15xf) - [Roundary Scan]	_ 🗆 X
Car Eile Edit View Operations Output	Debug Window Hele	
	G kg	
	F K!	
MPACT Provesses	Right click to Add Device or Initialize JTAG chain	
IMPACT Processes ↔ □ & ×		
	Boundary Scan	
Console		+□ & ×
<		>
Errors 🔔 Warnings	No Cable Co	nnection No File Open

**19)** When a device detected, click **Yes** to assign a configuration file.

``	ISE iMPACT (P.15xf) - [Boundary Scan] -						
😵 File Edit View Operations Output	Debug Window Help	- 8 ×					
🗋 🌶 🚽 🕒 🗄 🗰 🗮 🗖	<i>₽ №</i> ?						
PRACT Flows	Right click device to select operations SD/247 TDI Example TDI Example TDO Documentations TDO Documentations						
MPACT Processes ↔ ☐ ♂ × Available Operations are:	Auto Assign Configuration Files Query Dialog Do you want to continue and assign configuration files(3)? Don't show this message again, save the sating in preference. Ves No Identify Succeeded						
Console		⇔⊡ð×					
Identifying chain contense'0': : Manufactures's ID = Xilinx xo6slx8, Version : 2         // DIMFO:MRCM:1777 -         Reading C:/Xilinx/14.1/ISE_D5/ISE/spartan6/data/xe6slx8.bed         // INFO:MREACT:SO1 - '1': Added Device xc6slx8 successfully.							
Console Errors 🔬 Warnings	Configuration  Platform Cable USB  6 MHz	> usb-hs					

**20)** The generated configuration file is saved under the project directory. Locate the file and click **Open** to load it into the iMPACT software.

₿	ISE iMPACT (P.15xf) - [Boundary Scan]	- 🗆 🛛
🛞 File Edit View Operations Output D	ebug Window Help	_ 8 ×
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iMPACT Flows		
Boundary Scan     SystemACE     Create PROM File (PROM File Formatter)     WebTalk Data	TDI STUDEN xc6sk9 buoass Assian New Configuration File ? ×	
	Look in: 🎍 C: \Users \Adam \Desktop \XC65LX9 Mini Board Examples \Barrel_Shifter 🛛 🗸 🔇 🔇 🚺 🔃 🗐	
IMPACT Processes Available Operations are:	My Comp Adam Adam My Comp Adam JanAhead_run_1 xInx_auto_0xdb yd barrel_shifter.bit	
	Open —	
Identifying chain contents'0	File name:	
<pre>     INFO:iMPACT:1777 -     Reading C:/Xilinx/14.1/ISE_DS/I     INFO:iMPACT:501 - '1': Added De </pre>	Files of type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)	
	Cancel All	
done. PROGRESS_END - End Operation. Elapsed time = 0 sec.		
<		>
Console Serrors 🔬 Warnings	Configuration Platform Cable USB 6 MHz	usb-hs

**21)** When a message box appears and ask if you want to attach a SPI or BPI PROM. Click **No**. We will program the SPI flash later.

8	ISE IMPACT (P.15xf) - [Boundary Scan]	- 8 ×
File Edit View Operations Output Debug Winds	w Help	_ # ×
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MPACT Hows ++ C & X	Right click device to select operations	
Construction Sector (Construction)     Construction (Construction)     Construction (Construction)     Work Task Data	TO	
MPACT Processes ++		
Anabale Gopartions are	Attach SP or BID PDCM  This driver apport attached Flack PDCM. Dysou want watches SP or BPDCM to denice? Too Too Identify Succeeded	
	Boundary Scan	
Console		+- D # ×
'1': Loading file 'Ci/Users/Adam/Deaktop, done. JUNFO100FACT1225' - Startup Clock has been but the original bitstream file remains User1D read from the bitstream file - Ox Data width read from the bitstream file - UNFO10FEACT501 - '1': Added Device xeds.	XXSSIXW Humi Board Examples/Harrei Bhiffer/barrei mhiffer.bit' managed to 'JtagClk' in the bistreem stored in memory. TETTETT. * 1. * 8 successfully.	Î
<		×
Console 🔕 Errors 🔔 Warnings		
	Configuration (Platform C	able USB 6 MHz usb-hs

22) A Device Programming Properties window may pop up. Click OK.

8	ISE IMPACT (P.15xt) - [Boundary Scan]	- 8 ×
👺 File Edit View Operations Output Debug Window	w Help	_ <i>a</i> ×
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IPALCT Rose → C × → T Bondary Scin → D SystemACS → Create POM File (PBOM File Formatter) © Web144 Date	polyana To	
ØØ4CT Pressen Available Operations are	Device Programming Properties	
-	Boundary Scan	
Console		+- □ # ×
'1'LL Seding file 'CL/Gerz/Adam/Destrop/KO done. U. HFO:URACT.2257 - Disrup Clock has been o but the original histoream file remains uno Descilo read from the histoream file - OsFF Data width wasf from the histoream file - OsFF 0. University of the statement of the the 'LL of the statement of the statement of the statement of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the statement of the 'LL of the statement of the statement of the statement of the statement of the 'LL of the statement of the	XCHING Hani Band Eangler/Berel_Bhifter/Berel_mlifter.Bit* Ganged to "Papell" in the bitarream stored in mamory. schlagest #FTFFFF. ## successfully.	
📓 Console 🙆 Errors 🔔 Warnings	Configuration	Platform Cable USB 6 MHz usb-hs

23) Right-click the icon and select **Program** command. iMPACT will initiate the download process.

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Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Image: Constant Processes       Image: Constant Processes       Image: Constant Processes       Image: Constant Processes         Im	🛞 File Edit View Operations Output Debug Window	/ Help	- 6 ×
MPACT Processes     +     0     XV       Available Operations are:     +     0     X	🗋 🆻 🛃 🕺 🖓 🕼 🔭 📰 🇱 🛯 🏶 🚰 🗖	<i>₽</i> k?	
Bendary Scan     SystemAE     SystemAE     Create RROM File (PROM File Formatter)     Bendary     WebTalk Data     Set Device D     Get D	MPACT Flows ↔ □ 중 ×		
MPACT Processes         ↔ □ ♂ ×           Available Operations are         Set Programming Properties	다 말 한 Boundary Scen - 남 것(Find ACE - 급 Create PROM File (PROM File Formatter) 당 료 WebTalk Data	TDI Program Program TDO Barrier TDO Cone Step SVF Read Device DNA Add SV/RPI Flash	
Available Operations are: Set Programming Properties	MPACT Processes ++ □ = ×	Assign New Configuration File	
Program     Get Derice ID     Get Derice ID     Get Derice ID     Get Derice Signature/Usercode     Get Derice Status     Get Status	Available Operations are: Program G ct Device Signature/Usercode @ ct Device Status @ Che Status @ Ine Stap SIF One Stap SIF @ One Stap SIF @ One Stap SIF @ New Device DNA	Set Programming Properties Set Erase Properties Lunch file Assignment Wizard Set Target Device	
Boundary Scan		Boundary Scan	
Console ↔ D &	Console		⇔⊡₽×
<pre>'1': Loading file 'C:/UBers/Adam/Desktop/XCGSIX9 Mini Board Examples/Barrel_Shifter/barrel_shifter.bit' done. UFNF0:MEMCT:2257 - Startup Clock has been changed to 'JtagCIk' in the bitstream stored in memory, but the original bitstream file = mains unchanged UBersID read from the bitstream file = 0.4FFFFFFF. Data width read from the bitstream file = 1. UFNF0:MEMCT:501 - '1': Added Device xc6six9 successfully. </pre>	<pre>'1': Loading file 'C:/Users/Adam/Deskcop/3 done. U,INFO:MFACT:2257 - Startup Clock has been but the original bitstream file remains un UserEID read from the bitstream file = 0xFI Data width read from the bitstream file = U,INFO:MFACT:501 - '1': Added Device xofely </pre>	CGSIX9 Mini Board Examples/Barrel_Shifter/barrel_hifter.bit' changed to 'JtagClk' in the bitstream stored in memory, changed. FFFFFF. 1. 9 successfully.	~
🗄 Console 🔕 Errors 🔔 Warnings	🗐 Console 🙆 Errors 🔔 Warnings		
Configuration Platform Cable USB   6 MHz   usb-hs		Configuration Platform Cable USB 6 MH	z usb-hs

**24)** When programming is complete, the Program Succeeded message is displayed. Now, you can find only one LED is lit on board and rotating from left to right.

8	ISE	iMPACT (P.15xf) - [Boundary Scan	1	- D ×
Sile Edit View Operations Output	Debug Window Help			- 8
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MPACT Flows ↔ □				
Ter Te Boundary Scan → SystemACE → Create PROM File (PROM File Format ⊕ S WebTalk Data	TDI			
MDACT Processe + 미 취 X				
Available Operations are: Program G GP Device ID G GP Device (Signature/Usercode Read Device Status One Step SVF One Step SVF Read Device DNA		Program	Succeeded	
	<b>W</b>	Boundary Scan		
Console				+□ 8
<pre>U.INTO:IMPACT - 0011 1100 1110 U.INTO:IMPACT:579 - 1'1: Comple U.INTO:IMPACT:578 - '1': Comple U.E.K.yote = NOMMIC. LCK.yote = NOMMIC. U.INTO:IMPACT - '1': Checking d '1': Programmed successfully, PROGRESS_END - End Operation. Elapsed time = 1 sec.</pre>	1100 Sed downloading bit mming completed suc one pindone.	file to device. cessfully.		
				>
Console 💟 Errors 🔬 Warnings			Configuration	Platform Cable USB 6 MHz usb-hs

Note: In the previous steps, the configuration file is downloaded to the SRAM of the target device. As we know, SRAM is a kind of volatile memory, that means data stored in SRAM will be lost when power is removed. The XC6SLX9 Mini Board has a non-volatile SPI flash(W25Q64BV) to store the configuration file. Data will be automatically loaded into the SRAM of FPGA device during power up. The following steps will show you how to generate a PROM file and program it to the SPI flash.

25) Double-click Create PROM File( PROM File Formatter ).

2	ISE iMPACT (P.15xf) - [Bou	ndary Scan]			– 🗆 🗙
Sile Edit View Operations Output	Debug Window Help				- 8 ×
이 마이 아이	TDI xongeneration xongeneration too				
Available Operations are: Program Get Device D Get Device Status Read Device Status One Step SVF One Step SVF Read Device DNA	I	dentify Suc	ceeded		
	Boundary Scan				
Console					++⊡ & ×
<pre>[13] DONE PIN [14] SUSPEND STATUS [15] FALLBACK STATUS U.INPC.IMPACT.2219 - Status reg. U.INPC.IMPACT.2319 - Status reg. U.INPC.IMPACT.1539 - '1': Comple U.INPC.IMPACT.153 - '1': Program LCK_cycle = NoMait. U.INPC.IMPACT - '1': Checking di</pre>	ister values: 1000 eed downloading bit file to device. mming completed successfully. one pindone.	::	1 0 0		^
<pre>'1': Programmed successfully. </pre>					, ×
Console 🔇 Errors 🔔 Warnings			Configuration	Platform Cable USB 6 N	/Hz usb-hs

**26)** Select **Configure Single FPGA** in step1, 64M bit storage device in step 2, and change the **Output File Name** and **Output File Location** in step 3. Click **OK** to exit the setup window.

8		I	PROM Fi	le Formatter					×
Step 1. Select Storage Targe	t	Step 2.	Ade	Storage Device(s	)	Step 3.		Enter	Data
Storage Device Type : Xilinx Flash/PROM Non-Volatile FPGA		Storage Devi	<b>ce (bits)</b> ge Device	64M 🗸		General File Detail Checksum Fill Value	FF	Value	
SPIEash     Configure Single FPGA     Configure MultiBoot FPGA     BPI Flash     BIT Flash		64M	-			Output File Name Output File Location	Barrel_Shifter C:/Users/Adan	n/Desktop/XC6	SSLX 📂
Configure Single FPGA     Configure MultiBoot FPGA     Configure MultiBoot FPGA						Flash/PROM Fi	e Property	Value	
Generic Parallel PROM						File Format Add Non-Configura	tion Data Files	MCS No	<u> </u>
			ct PROM						
Description									
In this step, you will enter information to assist in settin • Checksum Fill Value: When data is insufficier • Output File Name: This allows you to specify • Output File Location: This allows you to spec- • Eile Format: DPOM files can be concreted in a	g up and g at to fill th the base i ify the dir ny numbe	generating a PR e entire memory name of the file rectory in which ac of inductor sta	OM file for t of a PROM to which yo the file nam	he targeted storage device a I, the value specified here is u ur PROM data will be written ed above will be created ate_Depending on the PROM	ind mode used to ca	alculate the checksur	n of the unused	portions.	s v

**27)** Add a device file as the source of this conversion. Locate the configuration file generated in previous steps.

₿		ISE iMPACT (P.15xf)	- [PROM File Formatter: SP	I Flash Single F	PGA]			3 ×
😼 File	Edit View Operations	Output Debug Window Help						- 8 ×
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IMPACT FI	lows	↔ □ ♂ ×						^
	Boundary Scan SystemACE Create PROM File (PROM File F WebTalk Data	Formatter)	0x0000_0000	(	<b></b>			
	2		Add Device					×
	🛞 🏵 🔻 🕯 🕨 T	his PC → Desktop → XC6SLX9 Mini Boa	rd Examples → Barrel_Shifter		v C	Search Barrel_Shifter		<u>م</u>
	Organize 🔻 New fold	ler				-		0
	^	Name	Date modified	Туре	Size			
iMPACT P Availabl	Homegroup     Homegroup     Homegroup     Desktop     Documents     Downloads     Music     Pictures     Videos	<ul> <li>Xil</li> <li>_ngo</li> <li>_xmsgs</li> <li>ipcore_dir</li> <li>iseconfig</li> <li>planAhead_run_1</li> <li>xlnx_auto_0xdb</li> <li>xst</li> </ul>	3/26/2015 9:00 AM 3/26/2015 9:03 AM 3/26/2015 9:04 AM 3/26/2015 8:41 AM 3/26/2015 8:43 AM 3/26/2015 9:03 AM 3/26/2015 9:03 AM 3/26/2015 8:48 AM	File folder File folder File folder File folder File folder File folder File folder				
Console	Local Disk (C:) FKBACK≢ 001 (E: Local Disk (F:) Local Disk (G:) Local Disk (H:) Ketwork	barrel_shifter.bit	3/20/2019 9:04 AM	BII File	333 KE	1		× ×
	File n	name: barrel_shifter.bit			~	FPGA Bit Files (*.bit)		~
						Open	Cancel	
								~
	La Caraca A Marca							>
Con	isole warn	migs	PROM File Generation Targe	t SPI Flash 0 Bits	used File: Untitle	ed in Location: C:\Xilinx\*	I4.1∨ u	ısb-hs

28) Double-click Generate File... command.

8	ISE iMPA	CT (P	.15xf	) - [P	ROM Fil	le Formatter:	SPI	Flash Single FPGA] -		×
🛞 File Edit View Operations Output Deb	ug Windov	v H	elp						_ 0	5 ×
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IMPACT Flows	⇔⊡ & ×	_					Т			^
Grand State     Soundary Scan     System ACE     System ACE     Create PROM File (PROM File Formatter)     Grand Read PROM File Pormatter)     Grand Read Read Read Read Read Read Read Rea					'el_shifte	0x0000_0000	8			
MPACT Processes	↔□♂×		PROM / FLAS	RevO				barre_sinner.or		
Available Operations are:			r				ŝ			
				Boi	undary Sca	0x000F_FFFF	è PR	IOM File Formatter: SPI Floch Strole FPGA		*
Consta										
Console									+-	8' X
FROM Name : IM FROM Size FROM Name : IM FROM Size '1': Loading file 'C://Jers/Adam. () INFO:IMFACT - Elapsed time = done. () INFO:IMFACT:501 - '1': Added Devi	: 104857 Report /Desktop// 1 sec. Loe xc6s1	6 bi1 KC6SJ K9 st	LX9 N	(ini ssfu:	Board	Examples/B	larr	el_Shifter/barrel_shifter.bit'		~
Add one device.532c1										~
<										>
📄 Console 🙆 Errors 🚹 Warnings										
PROM File Generation Target SPI Fla	sh 2,724,832	Bits u	sed	File: B	arrel_Shift	ter in Location: O	C:\Us	ers\Adam\Desktop\XC6SLX9 Mini Board Examples\Barrel_Shifter	/ usb-h	s .

**29)** The Generate Succeeded message is displayed when file is converted successfully.

8	ISE iMPA	CT (P	.15xf	) - (P	ROM Fil	le Formatter: S	PI Flash Single FPGA] -	□ ×
🎲 File Edit View Operations Output Del	ug Windo	v H	lp					_ 8 ×
🗋 🌶 🛃 🕼 🎞 🐲 😤 🖬 🥕 K?								
MPACT Flows	⇔⊡ & ×	_						^
Boundary Scan     SystemACE     SystemACE     Greate PROM File (PROM File Formatter)     B Create PROM File Verballe     WebTalk Data					el_shifte	0x0000_0000		
MPACT Processes Available Operations are:	↔ 🗆 🗗 X		PROM / FLASH	Rev0				
		0				0x000F_FFFF	Generate Succeeded	*
	,			Boi	undary Sca	n 😼	PROM File Formatter: SPI Flash Single FPGA	
Console								⇔⊡ð×
4. Add one device.532clINF0:IMPACT Total configuration bit size - 2 Total configuration bytes ice - 0x5327c (34064) bytes Loaded up Using uter-specified prom size o Niting file "Ci\Users\Adam\Desk Writing file "Ci\Users\Adam\Desk Writing file "Ci\Users\Adam\Desk	- Current 724832 b 340604 by from 0x0 f 1024K cop\XC6SL cop\XC6SL cop\XC6SL	time its. tes. X9 M: X9 M: X9 M:	ni l ni l ni l	/26/ Boar Boar Boar	2015 9: d Examp d Examp d Examp	19:28 AM Dles\Barrel_ Dles\Barrel_ Dles\Barrel_	Shifter/Barrel_Shifter.mcs". Shifter/Barrel_Shifter.prm". Shifter/Barrel_Shifter.cfi".	Ŷ
<								>
📄 Console 🙆 Errors 🔬 Warnings								
PROM File Generation Target SPI Fla	sh 2,724,83	2 Bits u	sed	File: B	arrel_Shift	ter in Location: C:	\Users\Adam\Desktop\XC6SLX9 Mini Board Examples\Barrel_Shifter/	usb-hs

**30)** Go to the Boundary Scan window and right-click on the icon, select Add SPI/BPI flash... command.

8	ISE iMPACT (P.15xf) - [Boundary Scan]	- 🗆 🗙
🛞 File Edit View Operations Output Debug Wine	ndow Help	- 8 ×
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MPACT Flows ↔ □ 🗗	×	
다. : The Soundary Sean - : A SystemACE - A Create PROM File (PROM File Formatter) 과 에 바라Talk Data	TDI Program Get Device ID xcc Get Device Signature Usercode barret_ One Step XVF TDO Read Device DNA ded SP/VEIP too ho	
	Assign New Configuration File	
MPACT Processes ++	× Set Programming Properties	
Program	Set Erase Properties	
Get Device ID	Launch File Assignment Wizard	
Read Device Status	Set Target Device	
One Step SVF     One Step SVF		
Read Device DNA		
	Boundary Scan 🛛 PROM File Formatter: SPI Flash Single FPGA	
Console		+□ & ×
		^
DAdd one device.532c1INFO:iMPACT - Current Total configuration bit size = 2724832	ent time: 3/26/2015 9:19:28 AM	
Total configuration byte size = 340604 b	bytes.	
0x5327c (340604) bytes loaded up from 0 Using user-specified prom size of 1024K	ix0	
Writing file "C:\Users\Adam\Desktop\XC63	SLX9 Mini Board Examples\Barrel_Shifter\Barrel_Shifter.mcs".	
Writing file "C:\Users\Adam\Desktop\XC63 Writing file "C:\Users\Adam\Desktop\XC63	SLX9 Mini Board Examples\Barrel_Shifter\Barrel_Shifter.prm".	
ALIOLING TILE OF (OBELS (RUBII (DESKOD) (NO.	Sans mini poura promptes (parter_birter_birter.orr .	
<		×
Console 🔕 Errors 🧘 Warnings		
	Configuration Platform Cable USB 6 M	MHz usb-hs

31) Locate the PROM file with .mcs suffix and click Open.

⊜ ⊝ ∽ ↑ 🌗 ⊦	XC6SLX9 Mini Board Examples → Barr	el_Shifter		v ¢	Search Barrel_Shifter		p
Organize 🔻 New fo	lder						0
☆ Favorites	Name	Date modified	Туре	Size			
Desktop	🕌 .Xil	3/26/2015 9:00 AM	File folder				
🐌 Downloads	🍑 _ngo	3/26/2015 9:03 AM	File folder				
😌 Dropbox	🎍 _xmsgs	3/26/2015 9:04 AM	File folder				
🔠 Recent places	퉬 ipcore_dir	3/26/2015 8:41 AM	File folder				
	퉬 iseconfig	3/26/2015 8:43 AM	File folder				
🛆 OneDrive	🎉 planAhead_run_1	3/26/2015 8:59 AM	File folder				
	🎉 xinx_auto_0_xdb	3/26/2015 9:03 AM	File folder				
🜏 Homegroup	🕌 xst	3/26/2015 8:48 AM	File folder		-		
	Barrel_Shifter.mcs	3/26/2015 9:19 AM	MCS File	915 KB			
🖳 This PC							
崖 Desktop							
Documents							
🗼 Downloads							
🔰 Music							
📄 Pictures							
🛃 Videos	<b>~</b>						
File	name: Barrel_Shifter.mcs			~	MCS Files (*.mcs)		~
					0.000	Canad	
					Open	Cancel	

**32)** Select the SPI PROM(W25Q64BV) and Data Width as shown below. Click **OK** to exit.

8	Select Attached SPI/BPI								
Se	elect the PROM attached to FPGA:	:							
	SPI PROM	✓ W25Q648V/CV	~						
	Data Width:	1	~						
	ОК	Cancel							

**33)** Right-click the icon and select **Program** command to start programming the on-board SPI flash.

8	ISE iMPACT (P.15x	f) - [Boundary Scan]	- 🗆 🗙
🎲 File Edit View Operations Output	Debug Window Help		_ 5 ×
🗋 ờ 🖬 🕹 🕼 🗙 🏭 📾 🔌 🔠	# # 🛷 📑 🖪 🥬 K?		
iMPACT Flows ↔ □	Right click device to select operations		
Boundary Scan     Boundary Scan     Gerear Piele 7     System ACE     Gerear PAON File (PROM File Format     Web Taik Data      MeMACT Processes     +-     d ×      Available Operations are:     Program     Verify     Bunk Check     Readback     Ger Device Checksum     Read Device Status	TDI Verify Eraze Blank Check Peradback. DO Asign New Configuratic Delete Set Frogramming Proper Set fase Properties. Edit Attached Flash Prop Launch File Azsignment Set Target Device	on File tries Wizard	
	Boundary Scan	PROM File Formatter: SPI Flash Single FPGA	
Console			++ ⊡ & ×
<pre>[13] DONE FIN [14] SUSPEND STATUS [15] FALLBACK STATUS [15] FALLBACK STATUS [1] INFO:IMFACT:2219 - Status reg [1] INFO:IMFACT:378 - '1': Complet [1] INFO:IMFACT:378 - '1': Complet [1] INFO:IMFACT:378 - '1': Complet [1] INFO:IMFACT:48 - '1': Complet [1] INFO:IMFACT - '1': Checking di [1] INF</pre>	ister values: 100 ted downloading bit file to dev mming completed successfully. one pindone.	: 1 : 0 : 0	^
Console Console Karnings		Configuration Platform Cable USB	6 MHz

34) Click **OK** when Device Programming Properties window appears.

8	ISE iMP/	ACT (P.15xf) - [Boundary Scan]		- 🗆 🛛
File Edit View Operations	Output Debug Window Help			- 5 ×
🗋 🆻 🛃  😹 🖺 💥 🖽 😫	) 🔉 🗉 🏭 🛷 📑 🔳 🥬 🌾			
IMPACT Flows	+ □ ♂ × Right click device to select operation	1		
Boundary Scan     D	Category	ning Properties - Device 1 Programmir	ng Properties X	
	- Device 1 (FPGA xc6slx9 )	Property Name	Value	
	Device 1 ( Attached FLASH, M2:	Verify	<b>v</b>	
		General CPLD And PROM Properties		
		Design-Specific Erase Before Programming	<b>v</b>	
MDACT Deserves		FPGA Device Specific Programming Properti	ies	
Augitable Operations are		After programming Flash	automatically load FPGA with Fla	
Program     Venfy     Erase     Blank Check     Readback     Get Device Checksum     Read Device Status	¢ >	<	cel Accily Heb	
Console				↔ 🗆 🗗 ×
<pre>[13] DONE PIN [14] SUSPEND STATUS [15] FALLBACK STATUS [16] FALLBACK STATUS [17] INFO: MPACT:2219 - Sta [17] INFO: MPACT:2219 - '1' [17] INFO: MPACT:719 - '1' [17] INFO: MPACT:718 - '1': LCK_cycle = NoWait LCK_cycle: NoWait</pre>	tus register values: 0 110 100 Completed downloading bit fil Programming completed success	: : : rully.	1 0 0	^
<pre>① INFO:iMPACT - '1': Che</pre>	cking done pindone.			~
< Frogrammed succes	ATULIV.			>
Console Console Wa	irnings		Configuration Platform Cable USB 6 MH	-Iz usb-hs

**35)** Wait patiently while programming the flash.

8	ISE iMPACT (P.15xf) - [Boundary Scan]	
😵 File Edit View Operations Output Debug Window	v Help	- 8 ×
🗋 🌶 🛃 🔌 緯 😂 🗢 🔚 🗇 🌾		
PPACF Flows     Constrainty Scan     ProvemAct     P	Right click device to velocit operations	
MPACT Processes ** 🗆 🗗 🗙	Configuration Operation Status	
,	Boundary Scan	
<pre>Console '1': IDCODE is 'ef4017' (in hex). '1': IDCOCE is 'ef4017' (in hex). '1': IDCOCE is 'ef4017' (in hex). '1': IDCODE is 'ef4017' (in hex). '1': Voing Sector Ense. '1': Voing Sector Ense. '1': Reading device contents</pre>		+ C & X
Console Console X Warnings	Configuration Platform Cable USB  6 MHz	> V

36) When programming is complete, the Program Succeeded message is displayed.

SE IMPACT (P.15xf) - [Boundary Scan]	- D ×
🛞 File Edit View Operations Output Debug Window Help	_ <i>B</i> ×
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MPACT Flows +	
Boundary Scan     System ACE     System ACE     WebTalk Data     Xotaba9     TD0     TD     Xotaba9     TD0     TD	
MPACT Processes + D & X	
Available Operations are Program Pierfy Bink Check Red Device Status Program St Program St Prog	icceeded
Boundary Scan	SPI Flash Single FPGA
Console	+□5×
<pre>unin reputer is a construction of the set of the s</pre>	Â
	v
	>
📋 Console 🥌 Errors 🔔 Warnings	Configuration Platform Cable USB 6 MHz usb-hs

In this section, we learned the procedure of creating a simple FPGA project and verified it on XC6SLX9 Mini Board. Maybe it's a boring journey. But i really hope you have had a basic understanding of FPGA design using ISE WebPACK. If you want to learn more, please read the help documents and application notes on Xilinx website.

# 4. Hardware

This section describes the hardware peripherals of the XC6SLX9 Mini Board in detail.

### Overview

The XC6SLX9 Mini Board is a pocket-sized platform for Xilinx Spartan 6 FPGA, it includes several basic components to learn digital design on FPGA.



#### XC6SLX9 Mini Board Block Diagram

## Peripherals and I/O Mapping

#### • LEDs

Eight LEDs are provided on this board. They are driven directly by the FPGA IOs. Setting one pin to high level lights the LED, and drive the pin low will turn it off. LEDs are usually used as status indicators. Also, eight LEDs can be used to display a 8-bit data.



LED	FPGA Pin Location
LD1	138
LD2	137
LD3	134
LD4	133
LD5	120
LD6	119
LD7	118
LD8	117

#### LED Interface

#### • Switches

The XC6SLX9 Mini Board includes two pushbuttons for user input. Because of the characteristic of mechanical contact switch, glitches will be generated when button is pressed or released. You can implement a debounce circuit on FPGA to filter out the noise. A 200ohm resistor is added to protect IOs from overcurrent damage when pins are set as output in low level. In this case, when button pressed, +3.3V will be shorted to GND via the internal transistor path, and damage the output buffer. In default, the button keeps in low level state, when pressed, it will transit to high level state. Release the button the state will return to low level.



#### Switch Interface

Switch	FPGA Pin Number	
SW1	132	
SW2	131	

#### • JTAG

The 14-Pin 2.54-Pitch JTAG header can be directly connected with a Xilinx download cable.



JTAG Connector	JTAG Connector	FPGA	Pin
Pin Number	Pin Name	Pin Number	Functionality
1	GND	—	GND
2	+3.3V	—	VCC
3	GND	—	GND
4	JTAG_TMS	107	TMS
5	GND	—	GND
6	JTAG_TCK	109	TCK
7	GND	—	GND
8	JTAG_TDO	106	TDO
9	GND	—	GND
10	JTAG_TDI	110	TDI
11	GND	—	GND
12	—	_	None
13	GND		GND
14	_	_	None

#### JTAG Interface

#### Clock Oscillator

Clock is an important element in synchronous digital circuit design. It's often used to synchronize the whole digital system. A 50 MHz oscillator is available on this board. You can use it as a global clock for your design or as a reference clock for internal PLL of FPGA.



#### **Clock Oscillator Interface**

Clock Oscillator	FPGA Pin Number	
Y1	50	

#### • USB to UART Bridge

Serial communication can be easily implemented and is widely used when data exchange is needed between PC and peripherals. Since most new generation PCs are not assembled with an older 9-Pin D-Sub serial port. But USB port is abundant. The USB to UART converter IC solves the problem while retaining the advantage of serial port. FT232R is used in this board to play a role of USB to UART converter. When the driver software is properly installed, it will function as a virtual serial port. In addition, two LEDs are used to indicate the status of the TXD and RXD data path. When valid data transfer is detected, the corresponding LED will blink.



UART Signal Name	FPGA Pin Number
FPGA_RX	47
FPGA_TX	46

#### • SPI Flash

The SPI flash on this board is intended to store FPGA configuration file. But it can also be used as a regular SPI flash if you like.



#### **SPI Flash Interface**

SPI Flash Signal Name	FPGA Pin Number	
CSO	38	
CCLK	70	
MOSI	64	
MISO	65	

#### • Expansion Header

Two groups of expansion header are available. Each header includes 36 I/Os and +5V, +3.3V power supply. The connector type is a 2x20 0.1" center-to-center, male.



Expansion Connector	Expansion Connector	FPGA	Pin Functionality
Pin number	Signal Name	Pin Number	
1	IO_P126	126	I/O
2	IO_P127	127	I/O
3	IO_P123	123	I/O

4	IO_P124	124	I/O
5	IO_P116	116	I/O
6	IO_P121	121	I/O
7	IO_P114	114	I/O
8	IO_P115	115	I/O
9	IO_P111	111	I/O
10	IO_P112	112	I/O
11	VIN	—	Power
12	GND	-	Ground
13	IO_P104	104	I/O
14	IO_P105	105	I/O
15	IO_P101	101	I/O
16	IO_P102	102	I/O
17	IO_P99	99	I/O
18	IO_P100	100	I/O
19	IO_P97	97	I/O
20	IO_P98	98	I/O
21	IO_P94	94	I/O
22	IO_P95	95	I/O
23	IO_P92	92	I/O
24	IO_P93	93	I/O
25	IO_P87	87	I/O
26	IO_P88	88	I/O
27	IO_P84	84	I/O
28	IO_P85	85	I/O
29	+3.3V	-	Power
30	GND	-	Ground
31	IO_P82	82	I/O
32	IO_P83	83	I/O
33	IO_P80	80	I/O
34	IO_P81	81	I/O
35	IO_P78	78	I/O
36	IO_P79	79	I/O
37	IO_P74	74	I/O
38	IO_P75	75	I/O
39	IO_P66	66	I/O
40	IO_P67	67	I/O

#### Header-J5 Interface



Expansion Connector	Expansion Connector	FPGA	Pin
Pin number	Signal Name	Pin Number	Functionality
1	IO_P45	45	I/O
2	IO_P44	44	I/O
3	IO_P43	43	I/O
4	IO_P41	41	I/O
5	IO_P40	40	I/O
6	IO_P35	35	I/O
7	IO_P34	34	I/O
8	IO_P33	33	I/O
9	IO_P32	32	I/O
10	IO_P30	30	I/O
11	VIN		Power
12	GND		Ground
13	IO_P29	29	I/O
14	IO_P27	27	I/O
15	IO_P26	26	I/O
16	IO_P24	24	I/O
17	IO_P23	23	I/O
18	IO_P22	22	I/O
19	IO_P21	21	I/O
20	IO_P17	17	I/O
21	IO_P16	16	I/O
22	IO_P15	15	I/O
23	IO_P14	14	I/O
24	IO_P12	12	I/O
25	IO_P11	11	I/O
26	IO_P10	10	I/O
27	IO_P09	09	I/O

28	IO_P08	08	I/O
29	+3.3V	—	Power
30	GND	_	Ground
31	IO_P07	07	I/O
32	IO_P06	06	I/O
33	IO_P05	05	I/O
34	IO_P02	02	I/O
35	IO_P01	01	I/O
36	IO_P143	143	I/O
37	IO_P142	142	I/O
38	IO_P141	141	I/O
39	IO_P140	140	I/O
40	IO_P139	139	I/O

#### **Revision History**

Revision	Date	Note	
REV. 0	10/1/2014	Initial release	
REV. 1	4/1/2015	Upgrade the on-board	
		SPI flash M25P80 to	
		W25Q64BV.	

# Thank You !